Analog Sequential Architecture for Neuro-Fuzzy Models VLSI Implementation

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Abstract: An analog sequential architecture for efficient neuro-fuzzy models implementation is proposed. The best features of digital and analog domains are combined to provide a high degree of flexibility (in terms of number of inputs, number of membership functions per input and number of fuzzy rules) when handling real world tasks. The performance estimations show a good area/throughput ratio, thus making the architecture suitable for a wide range of applications.

1. Introduction

Since the initial proposal of fuzzy set theory [1], because of its good behavior and easiness of implementation, it has been used in a wide range of applications, including among others, control, pattern recognition and signal processing. Different implementations of fuzzy systems have been proposed, including digital [2], [3], as well as analog [4], [5] alternatives.

In this paper we propose a novel analog sequential architecture which is able to combine the main features of digital and analog solutions, providing in this way an efficient alternative for the implementation of fuzzy models. Furthermore, by using some of the organization principles of an existing mixed analog-digital architecture [6], the resulting architecture will allow for the emulation of a wide range of artificial neural network models.

Our architecture has been developped to emulate the widely-used Sugeno fuzzy model [7], which states that the crisp output provided by the fuzzy system, *o*, is given by:

$$o = \frac{\sum_{i=1}^{P} \omega_i \cdot p_i}{\sum_{i=1}^{n} \omega_i} \tag{1}$$

$$p_i = \sum_{k=0}^{n} x_k \cdot c_k \tag{2}$$

where x_i are the crisp inputs to the system, n is the number of inputs, P is the number of fuzzy rules included in the fuzzy inference engine, ω_i is the value resulting from evaluating the i-th fuzzy rule and c_k is the proportionality coefficient for the k-th crisp input. x_0 equals to 1, so a constant c_0 can be added to the aggregation of the crisp inputs. The values of coefficients ω_i are evaluated as follows:

$$\omega_i = \min_{k=1}^{P}\left\{F_{i(k),x_k}\left(x_k\right)\right\} \tag{3}$$

where $F_{i(k),x_k}(.)$ is the membership function i for input x_k, and the number of fuzzy rules P can be n^m where m is the number of membership functions for each input.

2. The Proposed Architecture

The architecture proposed to emulate fuzzy models has been conceived to overcome the problems that arise with the natural mapping of each operation in a fully-parallel architecture, namely:

- *Exponentially-growing circuit size*. If all the rules are defined, then $P = n^m$, thus increasing in an exponential form with the number of inputs and membership functions.
- *Inefficiency*. The parallel architecture risks to be very inefficient if the number of inputs (n) and membership functions (m) of a given application do not match exactly the maximum value of n and m that the implementation could support.

The general organization of the proposed architecture is depicted in figure 1.

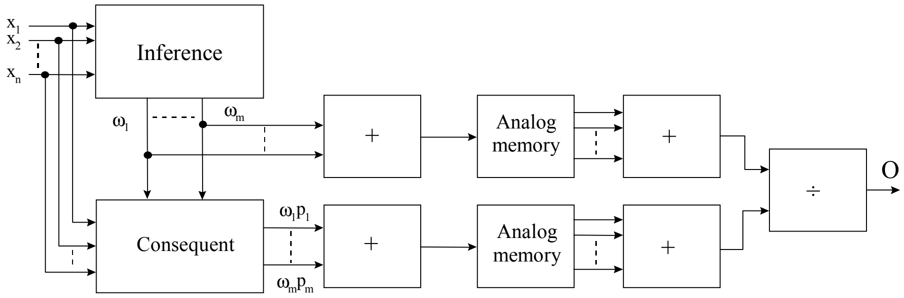

Figure 1. General organization of the proposed architecture

Five main building blocks can be identified. The *inference* block is in charge of evaluating the fuzzy rules (obtained as a *minimum* combination over the fuzzy values provided by determining the *m* fuzzy membership functions defined for each crisp input), while the *consequent* block weights these fuzzy rules with the linear combination of the inputs with the corresponding ω_i coefficients. The outputs provided by both blocks are given as analog currents. These currents are added and stored in analog memory cells. Block ÷ is in charge of yielding the final output, *o*, by calculating the division indicated in expression (1). The main function of the analog memory blocks is to store the partial results of the sequential calculations.

The basic principle used to emulate the Sugeno fuzzy model consists of obtaining at each emulation step as many fuzzy rules as membership functions are defined for each input variable. For this purpose, the *inference* block is organized as depicted in figure 2.

In this figure we have represented an example of the configuration for the *inference* block with 3 inputs (x_1, x_2, x_3) and 2 membership functions defined for each input. The blocks labelled $F_{k,xi}$ in the figure implement the k-th membership function for the i-th input, while the blocks labelled *Min()* provide at their outputs the minimum of their two input currents. The membership functions for the two first inputs are calculated sequentially, while those of the remaining input are calculated in parallel. Thus, at each emulation step two fuzzy rules comprising the 3 inputs are yielded. As a consequence, the 8 rules of the system are calculated in 4 emulation cycles. In a general case of a fuzzy system with *n* inputs and *m* membership functions defined per input, the inference block would provide the complete set of fuzzy rules in m^{n-1} cycles. The number of membership functions required is $m + n - 1$.

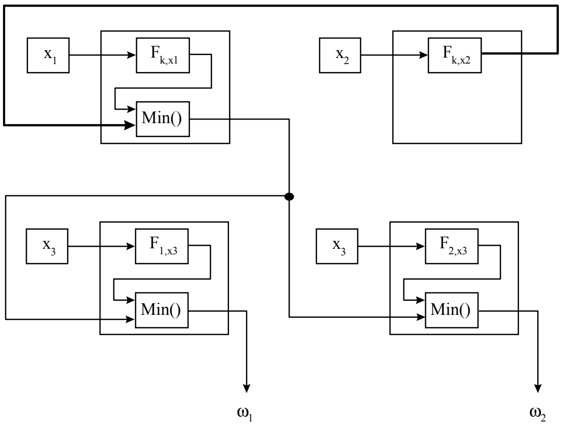

Figure 2. Organization of the *inference* block

The organization of the *consequent* block for the same example explained previously is depicted in figure 3.

The blocks labelled *$m_1()$* in this figure are analog-digital multipliers, while the blocks labelled *$m_2()$* are analog multipliers. The terms c_{ij} are the weight coefficients for the i-th input at the j-th emulation step, and can be stored in a digital memory. Since the structure used in this functional block is quite similar as that proposed in [6], it will be possible, with almost no control overhead, to use the proposed architecture to emulate also a wide range of neural models.

The organization and data flow proposed for the *inference* and *consequent* blocks is highly modular, allowing for the flexible emulation of different configurations for the fuzzy system. For instance, it can be demonstrated that a *inference* block composed of 6 basic cells and a *consequent* block integrated by 10 *$m_1()$* blocks and 5 *$m_2()$* blocks permit the emulation of the configurations stated in table 1 (parameterized in terms of number of inputs, n, and number of membership functions per input, m). A flexible architecture that can emulate all these configurations is shown in figure 4.

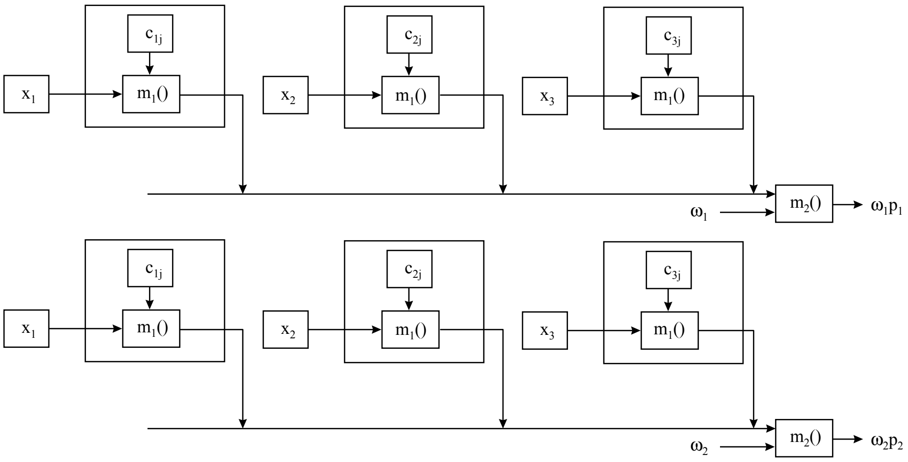

Figure 3. Organization of the *consequent* block

n	m
2	2
2	3
2	4
2	5

n	m
3	2
3	3
4	2

Table 1. Possible configurations for a system implemented with the proposed architecture

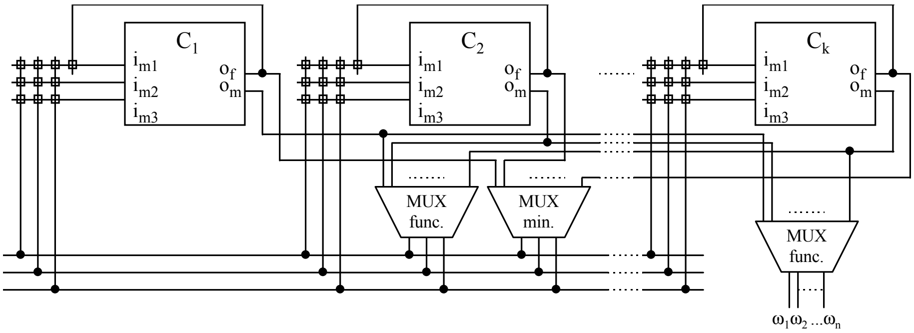

Figure 4. Configurable organization of the inference block

Table 2 summarizes the number of cells needed to implement a prototype architecture that emulates the fuzzy model configurations indicated in table 1.

	Number of cells	
	Example table 1	**General case**
Membership functions	6	m + n - 1
Min() functions (3-input)	6	m + n - 1
Analog-digital multipliers	10	2m
Analog multipliers	5	m
Analog memory cells	18	$n^{m-1} + 2$
Current adders (5-input)	4	2 (m inputs) + 2 (n^{m-1} inputs)
Current divider	1	1

Table 2. Summary of cells required to implement a prototype architecture

Furthermore, the capacity of the configuration memory required to organize the structure of the *inference* and *consequent* blocks, so as to adapt them to the particular requirements of the fuzzy model (number of inputs, and number of membership functions per input) has been estimated to be 119 bits. This configuration memory will be implemented as a shift register which will be loaded serially upon system power-up. As a consequence, bearing in mind also the low area demanded for the basic building blocks which constitute the proposed architecture, it can be considered as a good candidate for compact and flexible low cost applications.

3. Performance Estimation

As it was indicated in section 2, the *inference* block of the proposed architecture is able to produce at each emulation cycle as many fuzzy rules as membership functions are defined for each input. The worst case (obtained for the emulation of a 4-input, 2 membership functions per input fuzzy system) total execution delay, t_d, for the proposed architecture can be estimated by the following expression:

$$t_d = m^{n-1} \cdot (t_f + 3 \cdot t_{\min} + t_{mul} + t_{add} + t_{mem}) + t_{add} + t_{div} \qquad (4)$$

where t_f is the time required to evaluate a membership function, t_{min} is the time required to evaluate a *Min()* function, t_{mul} the time to evaluate an analog multiplication, t_{add} the time to evaluate a current addition, t_{mem} the settling time of the analog memory cell t_{div} the time required to evaluate a current division. Furthermore, since the basic cycle time is given by $(t_f + 3 \cdot t_{min} + t_{mul} + t_{add} + t_{mem})$, a quite conservative estimation for a 0.8 µm CMOS technology provides a maximum frequency for the system between 1 and 5 MHz, thus outperforming recent developments [4].

4. Conclusions And Future Work

In this paper we have addressed the hardware implementation of fuzzy models. By combining the solutions provided by analog and digital alternatives, we have proposed a novel analog sequential architecture whose main features are:

- The sequencing imposed to the basic functions to be performed and the modular organization permits a high degree of flexibility (in terms of number of inputs, membership functions per input and fuzzy rules) for emulating fuzzy models.
- The structural choice made for some of its functional blocks permits also the straightforward emulation of a wide range of artificial neural models.
- The concurrent execution scheme imposed in the data flow permits to attain a high processing speed, being therefore possible to handle real time applications.

Because of lack of space, the physical implementation of the building blocks has not been shown. However a careful selection of these blocks has been done and their interface compatibility has been analyzed. Therefore, architectural decisions were done bearing into mind the analog implementation issues.

Our current work is the detailed characterization of the basic cells which constitute the architecture for a 0.8 µm CMOS analog technology. Furthermore, a precision analysis is being performed in order to determine the programming scheme to be used for the membership function generator cells.

After this characterization process, a complete chip will be fabricated. This chip is intended to provide a physical solution for two very different real world tasks: the implementation of the control law in a DC-DC converter by means of fuzzy models and the implementation of the classification/decision engine to be included in a commercial automatic coin recognizer.

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