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# Novel Pulse-Width-Modulated Current-Mode Analog Defuzzifier for the Fuzzy Control of Switching DC-DC Converters

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**Abstract** - In this communication, the authors propose a current-mode analog circuit solution for the defuzzifying step required for the fuzzy-knowledge-based control (FKBC) of switching DC-DC converters. Considering the modulation of pulse widths which is needed for the control of switched power plants, the division operation at the output layer of a fuzzy inference controller takes advantage of the implicit signal-to-time conversion in the PWM process. This theoretical aspect is complemented with the proposal of a high-speed current-mode division circuit, which allows a wide range of switching frequencies. The PWM division circuit is preceded by a switched-current integrator to obtain a full defuzzifier. HSPICE layout-extracted transistor-level simulations for a standard CMOS 0.8 $\mu\text{m}$  technology verify the functionality of both the proposed defuzzifying method and circuit.

## I. INTRODUCTION

The idea of considering multidimensional nonlinear functions for the control of DC-DC switching power converters stands from the highly nonlinear nature of this kind of power processing systems. It is well-known that, in these circuits, the control signal consists of a pulsed waveform  $D(t)$ , pulse-width modulated, which, by driving the main power switch, switches the converter among the different linear sub-topologies it can acquire so as to obtain the required specifications.

On the other side, controller circuits based on the fuzzy inference process exhibit the property of allowing a multidimensional nonlinear mapping between the  $m$ -variable state-space vectors into a continuous control variable, thus implementing an intrinsically nonlinear MISO control. This nonlinear characteristic is obtained by means of subdivisions of the input space by placing locally tuned membership functions over the universe of discourse.

From both previous paragraphs, it can be stated that a controller based on the fuzzy set theory and its associated fuzzy inference process represents a plausible solution for the control of switching DC-DC power converters [14] and, in general, for power processing systems. This statement is mathematically supported by the recently demonstrated interpretation of FKBCs as universal function approximators.

Although having discussed the suitability of the fuzzy control, it should be emphasized the high processing complexity which this control, and, in turn, its associated implementation, require. Equation (1) shows the general expression that governs the fuzzy inference. A certain membership degree is associated with each variable  $x_k$  of the  $n$ -dimensional input vector  $x$ , through the membership function  $\Omega_{k,l}$  (related to the matching to a linguistic label). A fuzzy norm associated with the linguistic conjunction AND of each antecedent (usually minimum operation) applies to all the membership degrees thus obtaining the firing value  $w_r$  of the antecedent of this rule. On the other side, and considering the well-established Takagi-Sugeno (TS) inference method, the output hyperplanes  $d_i$  required to infer the conclusion via the generalized Modus Ponens, are obtained by weighted aggregation  $c_k$  weights of input variables.

$$o = f(\vec{x}) = \frac{\sum_{l=1}^M w_l T_l d_l}{\sum_{l=1}^M w_l T_l} = \frac{\sum_{l=1}^M \min_{k=1}^n \{\Omega_{k,l}(x_k)\} T_l \cdot \left( \sum_{k=1}^n x_k c_k^l \right)}{\sum_{l=1}^M \min_{k=1}^n \{\Omega_{k,l}(x_k)\} T_l} \quad (1)$$

As a last step, from all the theoretical methods relating the antecedents  $w_r$  with the consequents  $d_i$  to perform the defuzzification operation and hence obtaining a crisp continuous output variable  $o$ , the center-of-area method (COA) is considered, as it represents a well-proven trade-off between complexity and performance. It should be noted, however, that all other defuzzification methods, such as those operating with discrete information at the output layer [10], which are obtained for different values of the  $T_l$  weights [11] in equation (1), require the division operation. This operation is connatural to the fuzzy inference, representing a normalization of the contribution of each rule from the rule-base.

When considering the issue of the implementation of a FKBC, the use of a hardware controller circuit, as compared to its software-emulated counterpart, is more adequate since it features higher inference speed, thus allowing real-time fuzzy control. This high-speed inference is mandatory in the context of modern high-frequency switching converters, with switching frequencies up to 1MHz. Within the area of VLSI implementations, the analog design approach is a natural candidate as compared to a digital implementation. Analog designs inherently show higher speeds, more compact circuits in terms of area and power, as well as naturally allowing massively parallel processing and the implementation of fuzzy-related operations such as aggregations, scaling and nonlinear transfers.

## II. DEFUZZIFIER BY MEANS OF PWM

Several methods and circuits have been proposed in the literature for implementing the division operation within fuzzy controllers, although they are not particular to a specific control application. The design proposed in [1] performs the continuous-time division by means of a current-mode cell based on the translinear principle, which is related to 'true' current-mode operation of bipolar transistors or MOS transistors operated in subthreshold. Another approximation considers an algorithmic A-to-D converter as a mixed-signal division circuit with current-mode analog input signal and digital code output [2]. Other FKBC analog architectures [3] include weight normalization circuits, or normalization locked loops (NLLs) [22], prior to the aggregation stage, thus avoiding the division operation; however, this technique is not applicable when considering sequential-in-time architectures [4]. Recently, in [18], Dualibe *et al* propose a continuous-time division circuit by exploiting the linear characteristics of triode-region-operated MOS

transistors, driven by the signal levels imposed by a current-conveyor.

The proposal presented herein implements the analog division embedded in a generalized PWM scheme, thus avoiding redundant processing in the design of fuzzy controllers for PWM-driven power plants. Considering the classic scheme of pulse-width modulation (as shown in the first two time intervals in figure 1), the input signal  $s_N$  is continuously compared with a fixed-slope saw-tooth signal so as to obtain a pulsed and ON/OFF-modulated output signal. Allowing the ramp slope to be dependent on an additional input signal – denoted  $s_D$  in figure 1–, by integrating it for time intervals of duration  $T_s = 1/f_s$  equal to the PWM fundamental frequency, the expression describing the state change (the ON time,  $t_{ON}$ ) at the output of this two-input PWM modulator becomes:

$$s_N[k] = k_i \int_k^{k+t_{ON}} s_D[k] dt \Rightarrow t_{ON}[k] = k_i^{-1} \frac{s_N[k]}{s_D[k]} \quad (2)$$

$$\frac{t_k \leq t \leq t_{k+1}}{s_N[k]} \rightarrow s_N[k] = k_i s_D[k] t_{ON}$$

where  $s_N[k], s_D[k]$  are the input signals to the controller at the  $k$  instant, and  $k_i$  is the pulsed integrator proportionality constant. From this equation, the  $k$ -instant duty-cycle of the output waveform results in:

$$D_k = \frac{t_{ON}[k]}{T_s} = \frac{1}{k_i T_s} \frac{s_N[k]}{s_D[k]} \quad (3)$$

where the division operation appears explicitly. This division operation can be interpreted by virtue of the signal-to-time conversion performed by the pulse width modulation process.

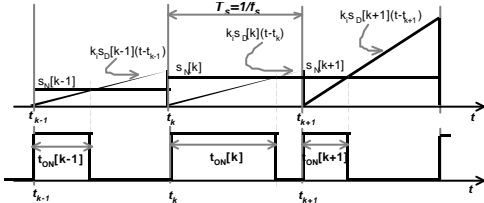


Fig 1. Time-domain representation of the pulse-width modulation process with signal-dependent ramp level.

For the sake of comparison, we note that there exist several well-known fuzzy and neural controller implementation proposals with signal representation by means of pulse width modulation [5], [6], [7]. However, they are proposed as hybrid circuits combining the advantages of both analog and digital designs, as for instance, and among other advantages, the ease to implement algebraic (addition, product) or logic (minimum) functions by digital circuits, and the robustness they present against interference and noise. Despite this PWM processing mode, these FKBC implementations consider complex division methods and circuits that do not take advantage of the implicit division which the PWM modulation provides, as shown in equation (3).

On the other hand, the use of PWM modulation as the processing core for product and division operations appears in [9], applied to continuous-time signals, consequently requiring lowpass filtering after the modulated signal so as to extract the DC-level of the pulse train. In this application, the PWM modulation is not considered by itself, but as a mean of obtaining highly linear products and divisions. At circuit level, the work in [9] proposes the use of switched capacitor techniques with voltage-mode circuits, which

precludes its use for high operation frequencies. Recently, the work presented in [16], presents a new concept of architecture for general signal processing and not only for soft computing, which merges analog and digital time-domain arithmetic operations in pulse widths, operating mainly in current-mode. The application of PWM techniques to realize various types of signal processing tasks has also been recently proposed in [20], where it is shown that these techniques are suitable to be configured as programmable VLSI circuits. Another related work is found in [19], where variable-level integration is considered to obtain time-sweeps and implement general Mamdani inference with output memberships, instead of TS singleton consequents.

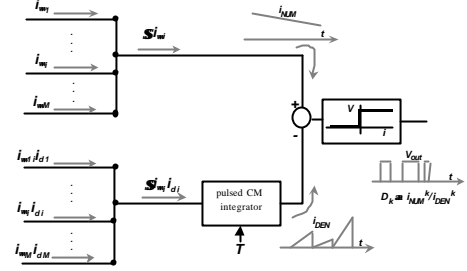


Fig 2. (a) Diagram of the proposed PWM defuzzification method

The imbrication of the PWM-division described by (3) in a complete defuzzifier scheme to perform the defuzzification operations expressed in (1) is depicted in fig.2. The figure depicts only the PWM defuzzification stage, and in this sense, it is considered that previous stages are in charge of obtaining the membership levels and their aggregations via t-norm operations to obtain each rule weight ( $i_w$ ), the Sugeno coefficients ( $i_d$ ) and the product among them ( $i_w i_d$ ). Note that the diagram already considers currents as information-carrying signals, as this is the natural mode of operation to obtain the multiple addition operation expressed in (1).

### III. CURRENT-MODE PWM DIVISION CIRCUIT

This section is devoted to the microelectronic implementation of the presented PWM-based division method. Figure 3 depicts the CMOS circuit proposed to implement the two-input PWM modulation and, hence, the division, operating with current-mode input signals and with ON/OFF PWM modulated output voltage signal. Note that, similarly to the continuous-time division circuit in [18], the signal representations fit defuzzifier applications. Namely, current-mode input signals to realize the signal additions and voltage-mode signals for off-chip communications; in addition the PWM division circuit has the advantage of delivering an ON/OFF signal that is appropriate for driving output pads.

The core of the PWM modulator circuit is constituted by a current-input voltage-output transimpedance high-speed comparator [8]. This comparator consists, by one side, of a digital inverter ( $M_{n,p\_inv}$ ), being its current-integrating capacitive input responsible for the comparator's high resolution. By the other side, a nonlinear feedback path is established between output and input nodes by means of a class AB voltage follower ( $M_{n,p\_fdb}$ ), which results, as required for current-mode operation, in a low-impedance node for the comparator. This comparator provides very short delay times, but this high-speed performance comes at the price of significant power consumption, which is about 1mW for the comparator circuit only. Being this a single-sided PWM modulation, however, a low-delay comparator is needed, since any delay impacts directly as an error on

the output duty cycle. Note that modulator input currents  $-I_N, I_D$  are buffered via two current mirrors ( $M_{Ni}, M_{No}, M_{Di}, M_{Do}$ ). The current integrator is composed of a transconductor (OTA), operated in open-loop, which detects and transduces the ramp voltage signal that is generated at the  $C_{int}$  capacitor due to the injection of  $I_D$  current. This configuration results in a current integration constant  $k_i = g_m/C_{int}$ , adjustable both by changing the capacitance value or electronically tunable via the OTA transconductance  $g_m$ . The value of the  $g_m/C_{int}$  factor has to be selected close to the switching period so as to obtain a reasonable margin of duty cycles in the PWM signal. The inverting input is taken as the transconductor input to obtain the inversion of the current required to perform the signal subtraction before the zero-crossing comparator. For the transconductor circuit, the class AB [12] linearized cell presented in [13], actually a pMOS-input version to detect low common-mode input signals, is considered. This circuit exploits the highly linear, electronically variable and high bandwidth transconductance that a pair of matched MOS transistors exhibit when the sum of their gate-source voltages are hold fixed.

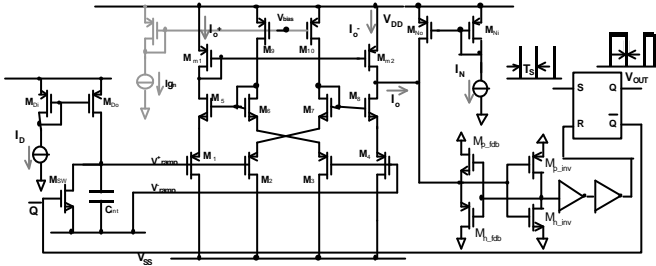


Fig 3. (a) Proposed current-mode CMOS circuit for the PWM division

The circuit proposed in [7] by El-Masry *et al.*, originally applied for the implementation of massively parallel neural networks, is similar to that of figure 3. In the former, however, neither the ramp level is variable since only products are to be implemented, nor the transconductor must preserve linearity, since the sigmoid-like transconductance characteristics are accounted for the post-synaptic nonlinear conformation required in artificial neural networks. A similar scheme is also recently proposed by Zeng *et al.* in [17], in the context of switched-current (SI) general nonlinear computing, but including a SI current integrator to generate current ramp signals. Another point that the PWM division circuit in fig. 3 features is a latched output and control of the reset action to the integrating capacitor, via a SR latch. This modification is included to avoid multistitching within one period, which is critical for power switch drive signals. In addition, for the test-chip prototype and taking into account nonideal implementation effects, offset compensating current mirrors have been included at the input node of the comparator in order to characterize the sensibility of the division operation to the OTA's offset.

The proposed PWM division circuit has been designed and laid-out using the  $0.8\mu\text{m}$  AMS CMOS analog technology, and simulations using layout-extracted circuits show proper operation. Figure 4a shows time-domain transistor-level HSPICE simulation results for the proposed PWM division circuit, from where it can be inferred, for continuous-time sinusoidal input current signals (upper traces), the expected operation of the circuit, in terms of speed and delay times. The second traces show both the OTA's output current, in where the linearity of the transconductor is qualitatively appreciated, and the input current to the comparator, both referred to the zero current-level. The bottom traces show the voltage-mode ON/OFF pulse train, and the voltage ripple level at the input of the transimpedance comparator. In order to evaluate the accuracy of the

implemented division operation, figure 4b shows a representation of the obtained duty cycles for a discrete sampling of the input space, as well as, superimposed, the theoretical hyperbolic curves associated with the division operation

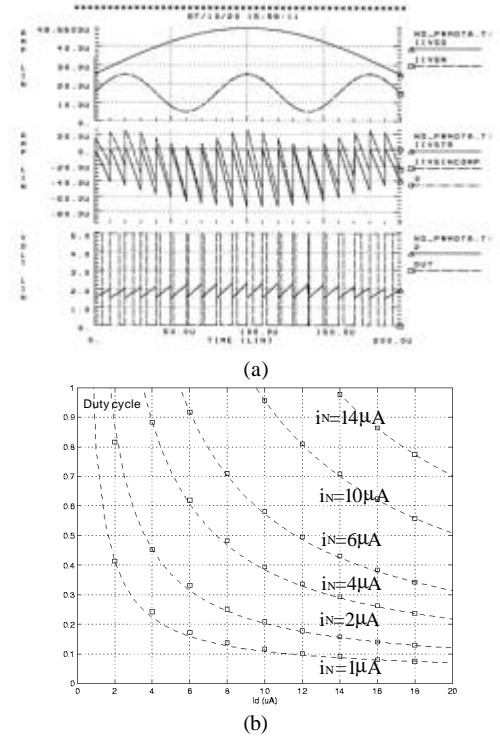


Fig 4. Simulation Results for the PWM division circuit (a) Time-domain behavior (b) Duty cycle as a function of  $I_N$  and  $I_D$

For illustration purposes, figure 5 depicts a sample layout of the current-mode PWM modulator, which occupies an area of about  $0.01 \text{ mm}^2$ .

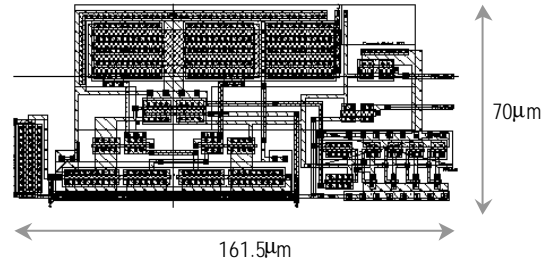


Fig 5. Layout of the current-mode PWM division circuit

#### IV. PWM SEQUENTIAL DEFUZZIFIER CIRCUIT

The previously described PWM division circuit has been embedded in a complete defuzzification circuit to be briefly described below. Considering the architecture principles proposed in [15], and their VLSI implementation [4], digitally-programmed analog building blocks sequentially provide current-mode discrete-time signals for both each rule-strength and its associated Takagi-Sugeno coefficient. This sequential operation constitutes a trade-off between area, throughput or inference speed, and circuit complexity, being possible to avoid exponentially growing circuits related to the so-called course of dimensionality [23]. A defuzzifier is in charge of obtaining the signal aggregations -short equation in (1)- and the division operation. Hence, in the sequential architecture context, we propose

the use of time aggregations (integrations) instead of the direct additions in fig. 2. The specific circuit design for this purpose is based on a switched-current discrete-time resettable accumulator depicted in fig. 6. Two of these circuits work in parallel for the numerator and denominator branch.

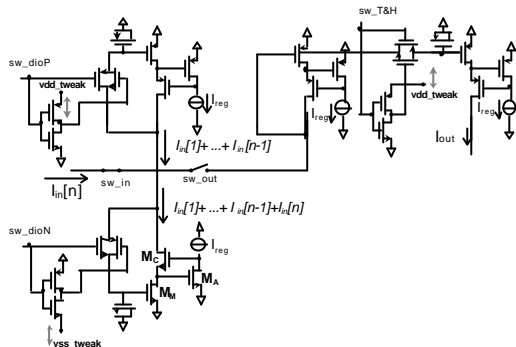


Fig 6. Switched-current complementary integrator

The circuit consists of a nMOS current-copier [24] to provide current sample memorization, properly followed by a complementary pMOS current-copier to provide, by accurate switching control, the required accumulation or discrete-time integration. Before a resetting signal occurs, and during the final accumulation cycle, the current is steered to a switched-current track&hold which contains the information of the numerator (or denominator) and drives the subsequent PWM division circuit. Several circuit techniques have been considered to alleviate the nonideal performance of second-generation current-copier cells, namely, cascode regulated techniques to reduce the effect of nonzero output conductances and complementary switches to reduce charge injection effects. The control circuit is based on a nonoverlapping two-phase clock generator that provides the control signals (shared by each accumulator). This circuit includes starved inverters [25] to obtain slow diode-opening switch control signals thus further reducing charge injection effects.

Note that, in [21], switched-current integration techniques have also been applied for defuzzifier purposes, being used in the context of the implementation of discrete output membership functions in Mamdani fuzzy controllers.

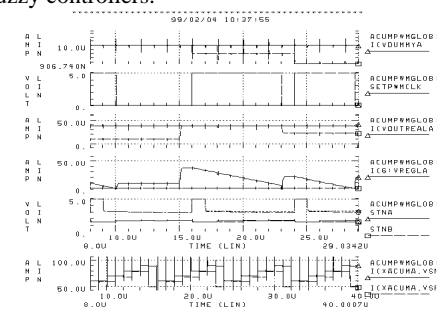


Fig 7. Global simulation results for the sequential switched-current current-mode PWM defuzzifier.

In order to validate the proper operation of the complete switched-current PWM defuzzifier, figure 7 depicts global simulation results. These simulations show input currents to the PWM division circuit (first and third plots), output pulsed voltage signal (second plot), current signal-dependent ramps involved in the PWM process (fourth plot), and voltages and current related to the switched-current accumulation stage (last two plots).

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