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Abstract

A mixed-signal VLSI circuit that efficiently maps the processing required for a Fuzzy Knowledge-Based Controller (FKBC) is presented. The proposed architecture is constituted by digitally-programmable continuous-time blocks to perform inference and switched-current memory cells to store in current-mode the partial information resulting from its pipeline operation. This FKBC is intended to provide multidimensional nonlinear-function approximation for switching power converters optimum control. Details of a new pulse-width-modulated defuzzification scheme are included. Transistor level post-layout simulation results for a 0.8 μm CMOS technology are included which validate the different blocks operation, their compatibility and the feasibility of the sequential architecture.

1. Introduction

FUZZY systems theory proposes a systematic method for mapping human knowledge into a multidimensional input-output nonlinear relation. Several real-world control engineering tasks require this universal approximation characteristic provided by fuzzy inference engines. In the application presented herein, the need for nonlinear control surfaces arises in the area of high-frequency switching-power converters, which are inherently nonlinear systems requiring highly nonlinear control laws. Thus, the need for high-frequency operation dictates the development of dedicated hardware implementation. The widely-accepted Sugeno [1] FKBC model is the best suited for implementation purposes, since it significantly reduces hardware complexity at the output defuzzification layer, using input-related output hyperplanes *in lieu* of output membership functions. The first-order Sugeno controller is described by the following IF-THEN rules:

$$\text{IF } x_1 \text{ is } \Omega_1^l \text{ and } \dots \text{ and } x_n \text{ is } \Omega_n^l \quad (1)$$

$$\text{THEN } d^l = c_0^l + c_1^l x_1 + \dots + c_n^l x_n$$

where Ω_i^l represent input fuzzy sets, c_i^l are constants and $l=1,2,\dots,M$ are the number of rules of the fuzzy processor. Given this inference core, and for a certain input vector $\bar{x} = (x_1, \dots, x_n)^T \in \mathfrak{R}^n$, the crisp output is computed using the discrete center-of-mass or weighted average method as:

$$o = f(\bar{x}) = \frac{\sum_{l=1}^M d^l w^l}{\sum_{l=1}^M w^l} \quad (2)$$

The activation degree values of each rule obtained in the antecedents are computed with the simplest connective t-norm

operation -i.e. minimum operator- over the membership degrees due to input membership functions $m_{\Omega_i^l}$, after

$$w^l = \min_{i=1}^n \{m_{\Omega_i^l}(x_i)\} \quad (3)$$

When the dynamics of the systems are known, as is the case for DC-DC switching converters, the analytical control law can be, in general, derived, and thus, there is an *a priori* knowledge of the law to be approximated by the FKBC. In this situation, the use of a neural-like algorithms to adjust or tune both the characteristics of membership functions –position over the universe of discourse, and slope- and the output first-order Sugeno coefficients may be used. The system being discussed will be trained with the ANFIS neuro-fuzzy learning algorithm proposed in [2].

Concerning the implementation of the FKBC, the signal processing mode of operation can either be digital [3], analog [4] or mixed analog/digital [5]. The speed constraints demanded by real-time control applications impose limits on digital implementations, and thus analogue versions of FKBC are the natural candidates for these tasks. Apart from the speed issue, compactness, low-area and low consumption also benefit the analogue counterparts, as well as the tolerance of trainable neurofuzzy systems to analogue implementation imperfections. Nevertheless, the neuro-fuzzy approach imposes the need of fully-adjustable processing blocks, thus precluding the use of implementations with fixed parameters. In this case, mixed-signal circuits consisting of analog processing cores with digitally-programmable characteristics, retain the flexibility and programmability of digital versions while being inherently faster and more compact due to their analog processing mode. The issue of interference coupling must be, however, addressed at the design phase.

2. FKBC Analogue Sequential architecture

The actual implementation of the controller consists of an analogue sequential architecture –depicted in fig 1(a)- which, concerning hardware complexity, efficiently maps the FKBC. There exist few examples of analogue sequential architectures in the neural networks implementation field [6], [7], but not in the area of fuzzy controllers. The main feature of the pipelined fuzzy controller, compared to its fully-parallel operation counterpart, is the capability of handling real-world control tasks, which present a considerable cardinality in number of fuzzy rules and input signals, while avoiding exponentially-growing circuit size [8]. In figures 1(b), 1(c) an example of the configuration for the inference block with 3 inputs (x_1, x_2, x_3) and 2 membership functions defined for each input and for the consequent block is represented. The blocks labeled F_{k,x_i} in the figure implement the k -th membership function for the i -th input, while the blocks labeled $Min()$ provide at their outputs the minimum of their two

input currents. The membership functions for the two first inputs are calculated sequentially, while those of the remaining input are calculated in parallel. Thus, at each emulation step two fuzzy rules comprising the 3 inputs are yielded. As a consequence, the 8 rules of the system are calculated in 4 emulation cycles. In a general case of a fuzzy system with n inputs and m membership functions defined per input, the inference block would provide the complete set of fuzzy rules $M=n^m$ in m^{n-1} cycles. The number of membership functions and Min operators required is $m + n - 1$. In figure 1(c), the blocks labeled $m1()$ are analog-digital multipliers, while the blocks labeled $m2()$ are analog multipliers. The terms c_{ij} are the weight coefficients of the output Sugeno hyperplanes for the i -th input at the j -th emulation step, and can be stored in a digital memory.

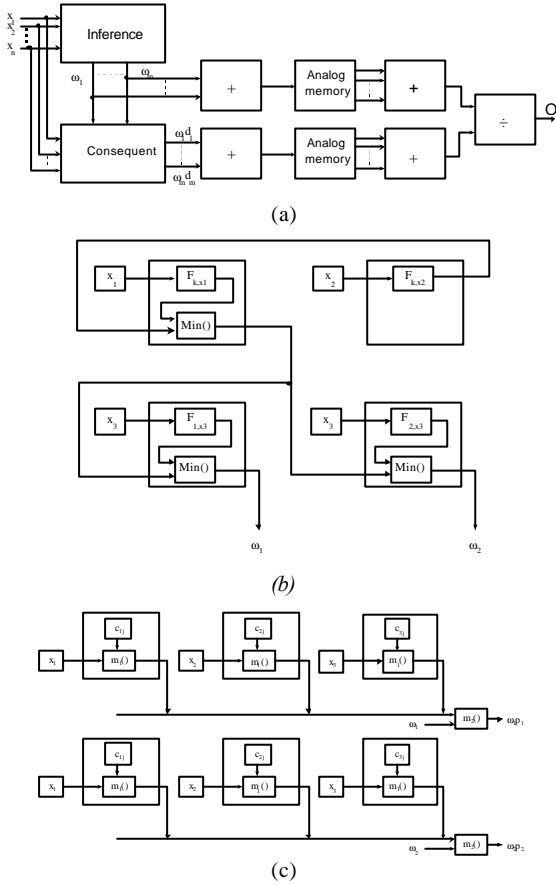


Figure 1. (a) Diagram of proposed FKBC analog sequential architecture [8] (b) Inference organization (c) Consequent organization.

3. Mixed-Mode VLSI Implementation Details

3.1. Inference Building Blocks

The VLSI implementation of the membership function -figure 2- takes advantage of the large-signal transconductance characteristics of two MOS transistor differential pairs to obtain the required bell-shaped function, inherently transconducting external voltage signals into current-mode signals. Both position and slope are digitally programmable with 6-bit resolution, being this resolution adequate for this closed-loop controller application. The use of transistor arrays as input compound transistors in the differential pairs makes their transconductance digitally tunable to adjust the slope of the characteristic transfer

function. For signal reflection and bias subtraction purposes, high-compliance one-stage cascode current mirrors are used [9]. These externally voltage-biased mirrors are used throughout the whole ASIC design to attain both high accuracy and copying precision while not reducing the operational margin of the blocks. Voltage offsets are applied at the differential pair to adjust the position of the membership transition region over the input voltage. These voltage levels are obtained by means of current-steering digital-to-analog converters biased with constant currents, which, in turn, are the main building blocks of the consequent part. Active current-voltage conversion is obtained with the I/V converter described in [10], based on a single nonlinearly-biased diode-connected MOS transistor.

Connective minimum operation circuits should be capable of accepting both voltage and current signal at their inputs and outputs for the proper operation of the inference block in fig 1(b). The natural aggregation property of current-mode operation is needed at the inference output, where the activation degrees w_i are to be summed. However, the internal signal transfer should be in voltage-mode. With this end, the MIN circuit used in [11] is adopted. This circuit applies a nonlinear signal compressing and subsequent decompressing at input and output ports, similar to the operation basis of a current mirror. At the internal nodes, the loser-takes-all property of a 2-inputs parasitic bipolar transistors differential pair is exploited, thus achieving the MIN operation:

$$I_{out} = f(V_{min}) = f(\min(f^{-1}(I_{in_1}), f^{-1}(I_{in_2}))) = \min(I_{in_1}, I_{in_2}) \quad (4)$$

Proper biasing for high-speed performance, level-shifting and cascoding is included in the MIN circuit.

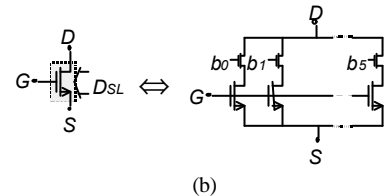
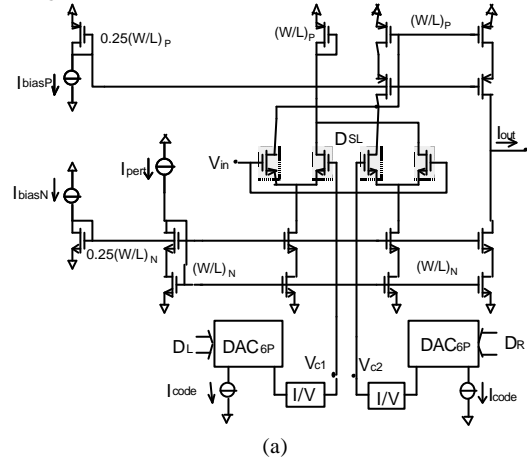


Figure 2. (a) VLSI design for the bell-shaped function. Detail of the transistor array used for digital slope adjustment.

3.2. Consequent Building Blocks

Concerning the consequent block, its operation is based on steering-current digital-to-analog converters using semi-algorithmic techniques -fig.3- [12], which operate as mixed-signal multipliers/weighters and, hence, implement the required

output hyperplane coefficients in the first-order Sugeno model. The use of a two-step algorithmic approach after,

$$I_{OUT} = I_{IN} \left(\left(\frac{b_{n-1}}{2} + \dots + \frac{b_n}{2^n} \right) + \frac{1}{2^2} \left(\frac{b_{n-1}}{2} + \dots + \frac{b_n}{2^n} \right) \right) \quad (5)$$

results in a significant reduction in area.

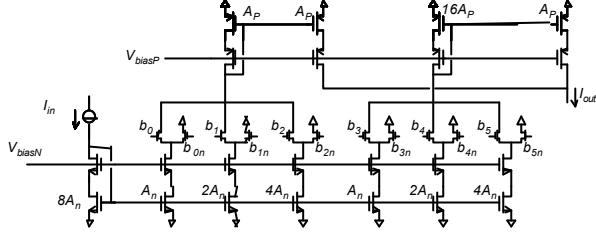


Figure 3. (a) Mixed-signal multiplier design based on high-frequency current-mode digital-to-analog converter.

The blocks labeled as $m_2()$ in figure 1(c) are in charge of implementing the analog current-mode product between activation degrees w^j and the output singletons d^l . A four bipolar transistor translinear cell has been designed for the hardware implementation of this current multiplier, for compactness and true current-mode operation reasons. This cell [13], naturally obtains current-domain products (6.2) in virtue of voltage summations around the so-called translinear loop (6.1) and silicon-junction exponential and logarithmic nonlinear relationships.

$$\sum_{k=1}^{k=N} nV_T \log \left(\frac{I_{Ck}}{I_{Sk}} \right) = 0 \Rightarrow \prod_{k=1}^{k=N} \frac{I_{Ck}}{I_{Sk}} = 1 \quad (6.1)$$

The shaded pnp bipolar transistors in figure 4 stand for parasitic lateral bipolar transistors available in standard CMOS technology. Although both current gain and Early voltages are low, the dynamic response is sufficient for this application ($f_T \sim 200\text{MHz}$). MOS-based regulating cascode techniques are applied at the multiplier's output transistor to lower output conductance to a negligible level.

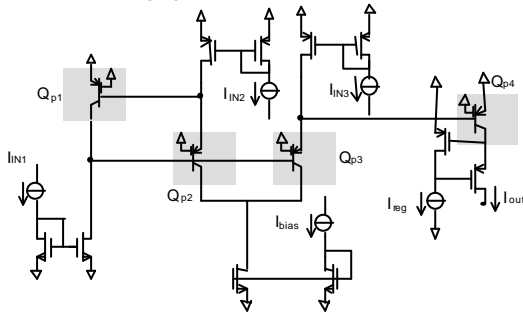


Figure 4. Diagram of the parasitic-bipolar translinear current-multiplier with regulated-cascode current output.

3.3 Switched-Current Storage Section and PWM time-domain division Blocks

Since the defuzzification method computes signal addition (2), the values of the rules w^j and the rule-weighted singletons $d^l w^j$ are sequentially delivered in current-mode by both inference and consequent branches, at the rate imposed by the system clock. The analog storing stage required by the sequential operation has been implemented using switched-current methods.

The storing core of this part of the circuit is the current copier, which is capable of loading and delivering a current sampler by storing its nonlinearly-related voltage sampler in a low-quality capacitor, available in digital single-poly technologies. Figure 5 shows a detailed schematic of the section comprising switched-current storing and subsequent division. At the switched-current stage, and for each branch –both numerator and denominator– the designed circuit features storing and discrete-time accumulating, by using complementary-type current copiers and proper switching control signals. For each m^{n-l} sequential cycles needed to perform the whole set of *IF-THEN* rules, an internal cycle is included to transfer the partial current sum stored at the main nMOS type current-copier to the pMOS type current-mirror. The accumulated signal at the k -th instant is:

$$i[k]_{NMOS} = i_{in}[k] + \sum_{j=1}^{k-1} i[j]_{PMOS} = \sum_{j=1}^k i[j]_{NMOS} \quad (7)$$

When all the emulation steps to obtain each rule are done, the final values of stored current are steered to current-mode sample-and-hold circuits, which will drive the following division stage. Simple cascode stages have been added to alleviate channel-modulation effects in the current copier [14]. The effects of charge injection and clock feedthrough have been minimized with the proper design of switch area and gate-shortened MOS storing capacitors for the corresponding frequency of operation.

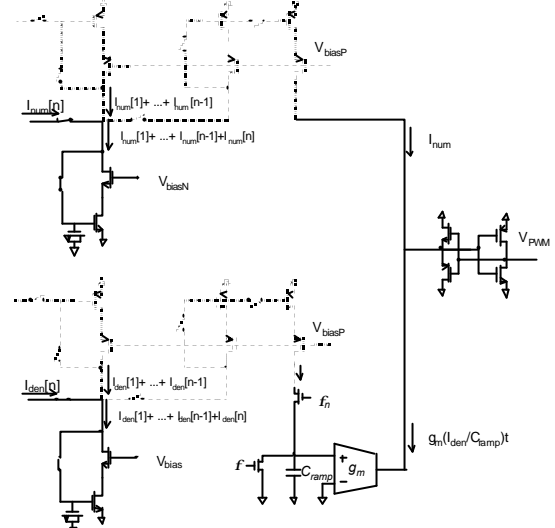


Figure 5. Diagram of the switched-current storing/integrating stage and PWM modulator.

Finally, the last stage features the capability of implementing the division operation required by the center-of-area defuzzification method, by means of the intrinsic division obtained by a PWM modulator, which is performed by virtue of its signal-to-time conversion. The resulting output signal for the FKBC is, thus, in voltage-mode and PWM modulated. This solution proposed by the authors, depicted in the righthand part of fig.5, is hardware-efficient and appropriate for the fully-integrated fuzzy control of switched power converters, or, in general, any power plant requiring a PWM drive. The circuit is based on the periodic integration of the current associated to the denominator (aggregation of rule values), thus creating a current-mode ramp signal with its peak level proportional to the signal. A current-input voltage-output high-speed comparator [15] compares continuously in time both numerator and denominator accumulated signals, being thus the duty cycle given by:

$$i_N^k = \frac{g_m}{C_{ramp}} \int_{kT_s}^{kT_s+t} i_D^k \cdot dt \xrightarrow{kT_s \leq t \leq (k+1)T_s} \frac{g_m}{C_{ramp}} \cdot i_D^k \cdot t$$

$$\Rightarrow D_k = \frac{t_{ON}}{T_s} = \frac{C_{ramp}}{g_m T_s} \frac{i_N^k}{i_D^k} \quad (8)$$

where the division operation appears in an explicit form.

4. Layout, Simulations and Results

The presented FKBC has been designed and laid-out using a 0.8µm CMOS analogue technology and simulations using extracted circuits show proper operation. As an example, figure 6 shows two performance validation results. Figure 6 (a) shows a post-layout simulation of the inference block including four membership functions and three MIN operators, programmed sequentially in position and slope but with saw-tooth input signal to show the membership characteristics over the whole input range. On the other hand, figure 6(b) illustrates, with a mixed circuit-level and behavioral-level sequential-mode simulation, the operation of the FKBC, showing the current-sample accumulation and PWM controller output signal. For illustration purposes, figure 7 corresponds to the layout of the digitally-programmable membership function circuit, including two current-steering semialgorithmic D/A converters and continuous-time I/V converters (bottom). The analog part of the dedicated controller features small size –about 0.7mm² for an eight-rule/three-input prototype testchip-, and low power consumption.

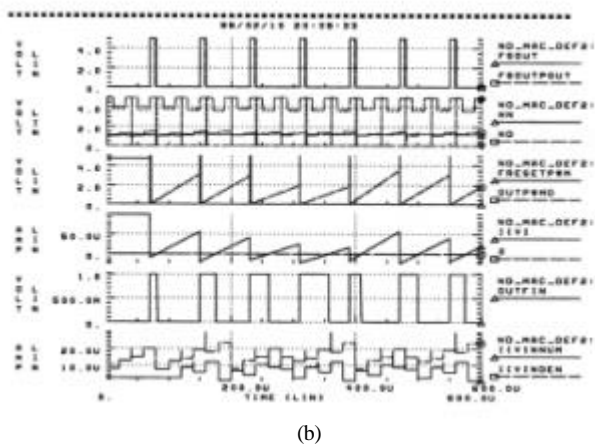
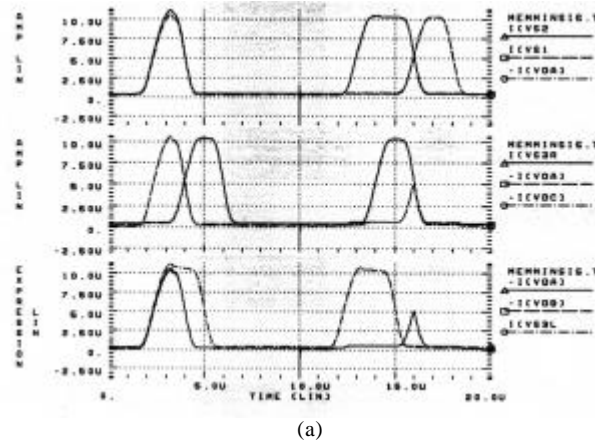


Figure 6. (a) Inference time-domain simulation (b) Discrete-time switched-current integration and PWM output waveforms.

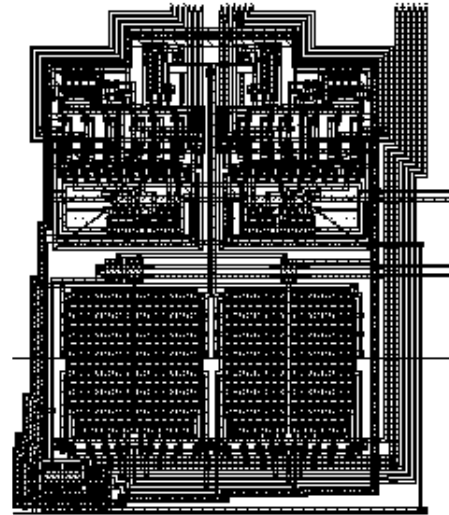


Figure 7. Designed layout for the fully-adjustable bell-shaped membership function. Dimensions shown in µm.

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