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TAKAGI-SUGENO NEUROFUZZY CONTROLLER**

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MIXED-SIGNAL IMPLEMENTATION OF A DISCRETE-TIME SEQUENTIAL TAKAGI-SUGENO NEUROFUZZY CONTROLLER

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ABSTRACT: This communication presents the design of a mixed-signal VLSI architecture that efficiently maps the processing required to emulate a Fuzzy Knowledge Based Controller (FKBC). At circuit level, the proposed FKBC is constituted by digitally-programmable analogue nonlinear blocks to perform inference, and switched-current memory cells to store in current-mode the partial information resulting from the sequential operation. Details of a novel pulse-width-modulated defuzzification scheme are included. Transistor-level post-layout simulation results for a 0.8µm CMOS technology are included which validate the operation of the different blocks, their compatibility and the feasibility of the sequential architecture. This FKBC is intended to provide multidimensional nonlinear-function approximation for switching power converters control.

INTRODUCTION

Fuzzy systems theory proposes a systematic method for mapping human knowledge into a multidimensional input-output nonlinear relation. Several real-world control engineering tasks require this universal approximation characteristic provided by fuzzy inference engines. In the application presented herein, the need for nonlinear control surfaces arises in the area of high-frequency switching power converters, which are inherently nonlinear systems requiring highly nonlinear control laws. Thus, the need for high-frequency operation dictates the development of dedicated hardware implementation. The widely-accepted Takagi-Sugeno (TKS) [1] FKBC model is the best suited for implementation purposes, since it significantly reduces hardware complexity at the output defuzzification layer, using input-related output hyperplanes in place of output membership functions. The first-order TKS fuzzy controller is described by the following set of IF-THEN rules:

$$\begin{aligned} & \text{IF } x_1 \text{ is } \Omega_1^l \text{ and } \dots \text{ and } x_n \text{ is } \Omega_n^l \\ & \text{THEN } d^l = c_0^l + c_1^l x_1 + \dots + c_n^l x_n \end{aligned} \quad (1)$$

where Ω_i^l represent input fuzzy sets, c_i^l are constants which define the consequent hyperplanes, and $l=1,2,\dots,M$ are the number of rules of the fuzzy processor. Given this inference core, for a certain input vector $\vec{x} = [x_1, \dots, x_n]^T$, and when considering the minimum operation as the connective *and*, the crisp output is computed using the discrete center-of-mass or weighted average method as:

$$o = f(\vec{x}) = \frac{\sum_{l=1}^M w_l d_l}{\sum_{l=1}^M w_l} = \frac{\sum_{l=1}^M \min_{k=1}^n \{F_{l(k),x_k}(x_k)\} \left(\sum_{k=1}^n x_k c_k^l \right)}{\sum_{l=1}^M \min_{k=1}^n \{F_{l(k),x_k}(x_k)\}} \quad (2)$$

where F_{l,x_k} stand for the membership functions associated to the Ω_k^l fuzzy set.

When the dynamics of the systems are known or capable of being modelled, as is the case for DC-DC switching converters, the analytical control law can be, in general, derived, and thus, there is an *a priori* knowledge of the nonlinear law to be approximated by the FKBC. In this situation, the use of neural-like algorithms to adjust or tune both the characteristics of membership functions –position over the universe of discourse, and slope- and the output first-order Sugeno coefficients may be considered [18]. The system being discussed will be trained with the ANFIS neuro-fuzzy learning algorithm proposed in [2], by making use of chip-in-the-loop techniques in order to account, at the training phase, for implementation non-idealities.

Concerning the implementation of the FKBC, the signal processing mode of operation can either be digital [3], analogue [4] or mixed analogue/digital [5]. The speed constraints demanded by real-time control applications impose limits on digital implementations, and thus analogue versions of FKBC are the natural candidates for these tasks. Apart from the speed issue, compactness, low-area and low consumption also benefit the analogue counterparts, as well as the tolerance of trainable neurofuzzy systems to analogue implementation imperfections. Nevertheless, the neuro-fuzzy approach imposes the need of fully-adjustable processing blocks, thus precluding the use of implementations with fixed parameters. In this case, mixed-signal circuits consisting of analogue processing cores with digitally-programmable characteristics, retain

the flexibility and programmability of digital versions while being inherently faster and more compact due to their analogue processing mode. The issue of interference coupling must be, however, addressed at the design phase. Lastly, although the approach investigated here is based, as stated, on a mixed analogue-digital architecture, promising results have also been obtained when exploiting the analogue storing capabilities of floating-gate transistors [19],[20].

FKBC ANALOGUE SEQUENTIAL ARCHITECTURE

Real-world control tasks require high cardinality of inputs, granularity of input space and number of rules. In this sense, it should be stated that existing FKBC implementation architectures lack sufficient number of fuzzy rules, because of the so-called 'course of cardinality', which in practice results in area-consuming VLSI circuits.

The actual implementation of the proposed controller consists of an analogue sequential architecture, depicted in fig 1(a), which, concerning hardware complexity, efficiently maps the FKBC. There exist some examples of analogue sequential architectures in the neural networks implementation field [6], [7], but not in the area of fuzzy controllers. The main feature of the sequential fuzzy controller, compared to its fully parallel operation counterpart, is the capability of avoiding exponentially-growing circuit size [8]. Table I summarises the hardware complexity in terms of the degree of sequentiality. An n -dimensional input space, with a granularity of m membership functions per input dimension, and the associated m^n rules are considered as the general description of the operation of the fuzzy controller.

| | index | memberships | time cycles | outputs |
|----------------|-----------------------|---------------------------------|-------------------------|-------------------------------|
| sequential | n | n | m^n | 1 |
| mixed s/p | $n-1$ | $(n-1)+m^1$ | m^{n-1} | m |
| mixed s/p | $n-2$ | $(n-2)+m^2$ | m^{n-2} | m^2 |
| | ... | ... | ... | ... |
| | 1 | $1+m^{n-1}$ | m^1 | m^{n-1} |
| fully parallel | 0 | m^n | 1 | m^n |
| general | i | $i+m^{(n-i)}$ | m^i | $m^{(n-i)}$ |

Table I. Architecture complexity as a function of the degree of sequentiality.

Concerning the testchip under consideration, which is a 3-input and 2-membership-functions per input FKBC, an architecture exhibiting a certain degree of sequentiality (complexity over time) and parallelism (complexity sprout over area) is considered (shaded row in table I). This architecture delivers $2^2=8$ fuzzy rules, 2 per step, in 4 emulation steps. In figures 1(b), 1(c) the configuration for the inference block with 3 inputs (x_1, x_2, x_3) and 2 membership functions defined for each input and for the consequent block is represented. The blocks labelled

$F_{k,xi}$ in the figure implement the k -th membership function for the i -th input, while the blocks labelled $Min()$ provide at their outputs the minimum of their two input signals. The membership functions for the two first inputs are calculated sequentially, while those of the remaining input are calculated in parallel. Thus, at each emulation step two fuzzy rules comprising the 3 inputs are yielded. As a consequence, the 8 rules of the system are calculated in 4 emulation cycles. In a general case of a fuzzy system with n inputs and m membership functions defined per input, the inference block would provide the complete set of fuzzy rules $M=n^m$ in m^{n-1} cycles. The number of membership functions required is $m + n - 1$. In figure 1(c), the blocks labelled $m_1()$ are analogue-digital multipliers, while the blocks labelled $m_2()$ are analogue multipliers. The terms c_{ij} are the weight coefficients of the output Sugeno hyperplanes for the i -th input at the j -th emulation step, and are stored, as well as the coefficients defining $F_{k,xi}$, in a digital memory.

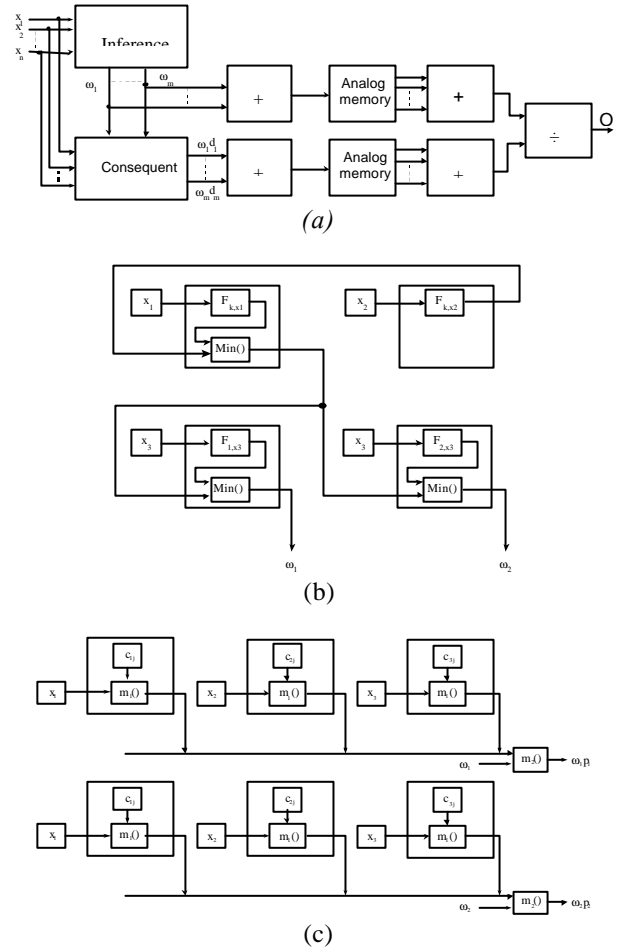


Figure 1. (a) Diagram of proposed FKBC analogue sequential architecture [8] (b) Inference organisation (c) Consequent organisation.

MIXED-MODE VLSI IMPLEMENTATION DETAILS

Inference Building Blocks

The VLSI implementation of the membership function - figure 2- takes advantage of the large-signal transconductance characteristics of two MOS-transistor differential pairs to obtain the required bell-shaped function, inherently transconducting external voltage signals into current-mode signals. Both position and slope are digitally programmable with 6-bit resolution, being this resolution adequate for this closed-loop controller application. The use of transistor arrays as input compound transistors in the differential pairs makes their transconductance digitally tuneable to adjust the slope of the characteristic transfer function. For signal reflection and bias subtraction purposes, high-compliance one-stage cascode current mirrors are used [9]. These externally voltage-biased mirrors are used throughout the whole ASIC design to attain both high accuracy and copying precision while not reducing the operational margin of the blocks. Voltage offsets are applied at the differential pairs to adjust the position of the membership transition region over the input voltage. These voltage levels are obtained by means of current-steering digital-to-analogue converters biased with constant currents, which, in turn, are the main building blocks of the consequent part. Active current-voltage conversion is obtained with the I/V converter described in [10], based on a single nonlinearly-biased diode-connected MOS transistor.

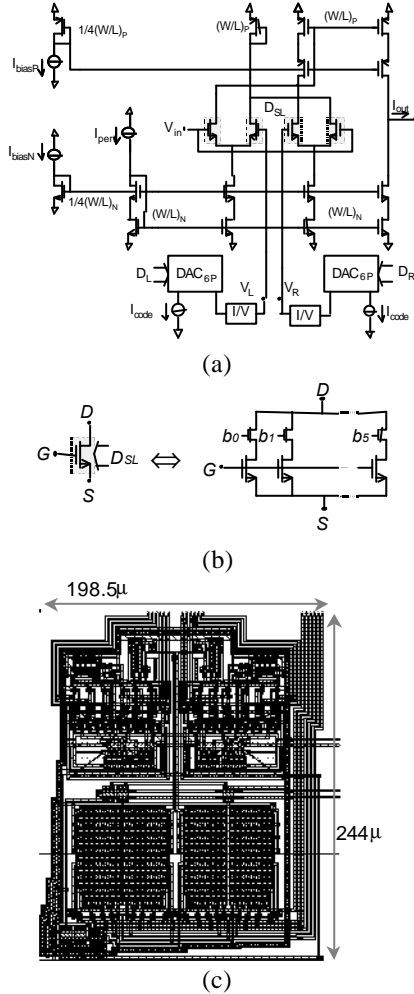


Figure 2. (a) VLSI design for the bell-shaped function. (b) Detail of the transistor array used for digital slope adjustment (c) sample layout

For illustration purposes, figure 2(c) corresponds to the layout of the digitally-programmable membership function circuit, including two current-steering semi-algorithmic D/A converters and continuous-time I/V converters (upper half of the figure).

Connective minimum operation circuits should be capable of accepting both voltage and current signal at their inputs and outputs for the proper operation of the inference block in fig 1(b). The natural aggregation property of current-mode operation is needed at the inference output, where the activation degrees w are to be summed. However, the internal signal transfer should be in voltage-mode. With this end, the MIN circuit used in [11] is adopted (figure 3). This circuit applies a nonlinear signal compressing (nonlinear function f^{-1}) and subsequent decompressing (f) at input and output ports, similar to the operation basis of a current mirror.

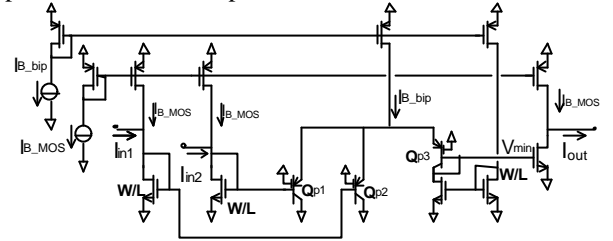


Figure 3. (a) Current/voltage-mode minimum circuit.

At the internal nodes, the loser-takes-all property of a 2-inputs parasitic bipolar transistors differential pair is exploited, thus achieving the MIN operation:

$$I_{out} = f(V_{min}) = f(\min(f^{-1}(I_{in1}), f^{-1}(I_{in2}))) = \min(I_{in1}, I_{in2}) \quad (4)$$

Proper biasing for high-speed performance, level-shifting and low-voltage cascoding is included in the MIN circuit.

Consequent Building Blocks

Concerning the consequent block, its operation is based on steering-current digital-to-analogue converters using semi-algorithmic techniques [12], which operate as mixed-signal multipliers/weighters and, hence, implement the required output hyperplane coefficients in the first-order TKS model. The use of a two-step algorithmic approach after

$$I_{OUT} = I_{IN} \left(\left(\frac{b_{n-1}}{2} + \dots + \frac{b_{n-1}}{2^2} \right) + \frac{1}{2^2} \left(\frac{b_{n-1}}{2} + \dots + \frac{b_0}{2^2} \right) \right) \quad (5)$$

results in a significant reduction in area. Figure 4(a) depicts the actual 6 bit low-voltage current-steering DAC used in the sequential fuzzy controller.

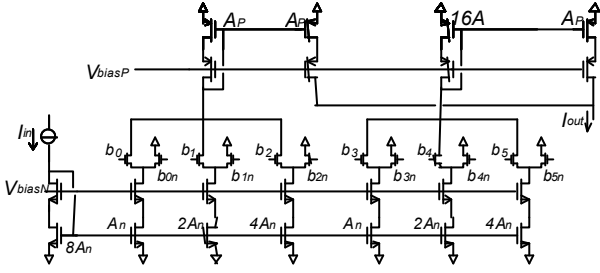


Figure 4. (a) Mixed-signal multiplier design based on high-speed current-mode digital-to-analogue converter.

The blocks labelled as $m_2()$ in figure 1(c) are in charge of implementing the analogue current-mode product between rule activation degrees ψ and the output singletons d^l . A four bipolar transistor translinear cell has been designed for the hardware implementation of this current multiplier, for compactness and true current-mode operation reasons. This cell [13], naturally obtains current-domain products (6) by virtue of voltage summations around the so-called translinear loop and silicon-junction exponential-like nonlinear relationships.

$$I_{OUT} = \frac{I_{in1} \cdot I_{in2}}{I_{in3}} \quad (6)$$

The shaded pnp bipolar transistors in figure 5 stand for parasitic lateral bipolar transistors available in standard CMOS technology. Although both current gain and Early voltages are low, the dynamic response is sufficient for this application ($f_i \sim 200\text{Mhz}$). MOS-based regulating cascode techniques are applied at the multiplier's output transistor to lower output conductance to a negligible level.

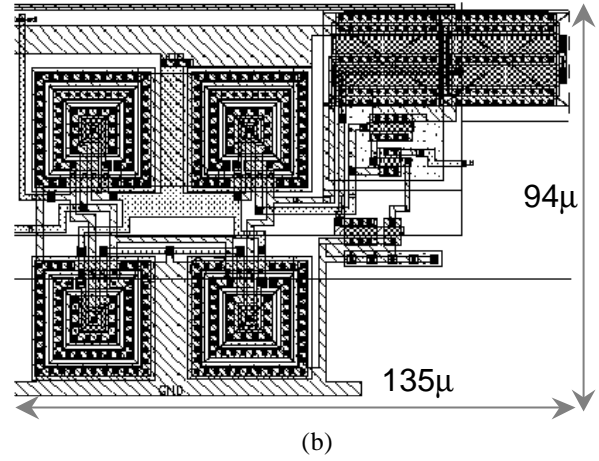
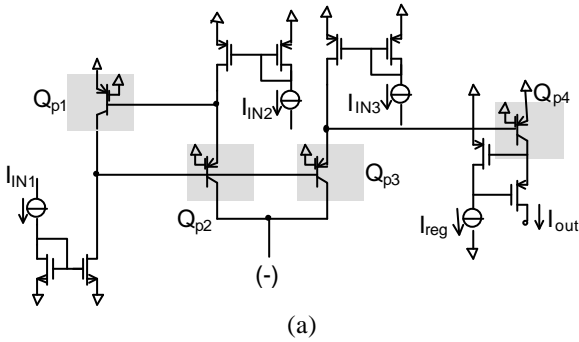


Figure 5. (a) Diagram of the parasitic-bipolar translinear current-multiplier with regulated-cascode current output. (b) Sample layout

Switched-Current Storage Section and PWM time-domain division Blocks

Since the defuzzyfication method computes signal addition (2), the values of the rules ψ and the rule-weighted singletons $d^l \psi$ are sequentially delivered in current-mode by both inference and consequent branches at the rate imposed by the system clock. Therefore, the controller features accumulation or discrete-time integration instead of concurrent aggregation. At circuit level, the analogue storing-integrating stage required by the sequential operation has been implemented using switched-current (SI) methods. The storing core of this part of the circuit is the current copier [14], which is capable of loading and delivering a current sampler by storing its nonlinearly-related voltage sampler in a low-quality capacitor, available in digital single-poly technologies. Figure 6(a) shows a detailed schematic of the section comprising switched-current processing. For each branch –both antecedent and consequent currents– the designed circuit features storing and discrete-time accumulating, by using complementary-type current copiers and proper switching control signals. For each m^{n-1} sequential cycles needed to perform the whole set of *IF-THEN* rules, an internal cycle is included to transfer the partial current sum stored at the main nMOS type current-copier to the pMOS type current copier. The accumulated signal at the k -th instant is:

$$i[k]_{NMOS} = i_{in}[k] + \sum_{j=1}^{k-1} i[j]_{PMOS} = \sum_{j=1}^k i[j]_{NMOS} \quad (7)$$

When all the emulation steps to obtain each rule are done, the final values of stored current are steered to current-mode sample-and-hold circuits, which will drive the following division stage. Regulated cascode stages have been added to alleviate channel-modulation effects in the current copier. The effects of charge injection and clock feedthrough have been minimised with the proper design of switch area and gate-shortened MOS storing

capacitors for the corresponding frequency of operation. A charge injection compensation scheme, to be further described in a future communication, is included which uses a pMOS transistor M_{p1} with variable activation voltage to tweak the charge injected by the diode-closing transistor M_{n1} . In order to properly control this SI integrator, a non-overlapping three-phase control signals generator is included in the design. This clock generator makes use of one-side starved digital inverters to obtain slow diode-opening waveforms with adjustable decay time, as shown in figure 6(b).

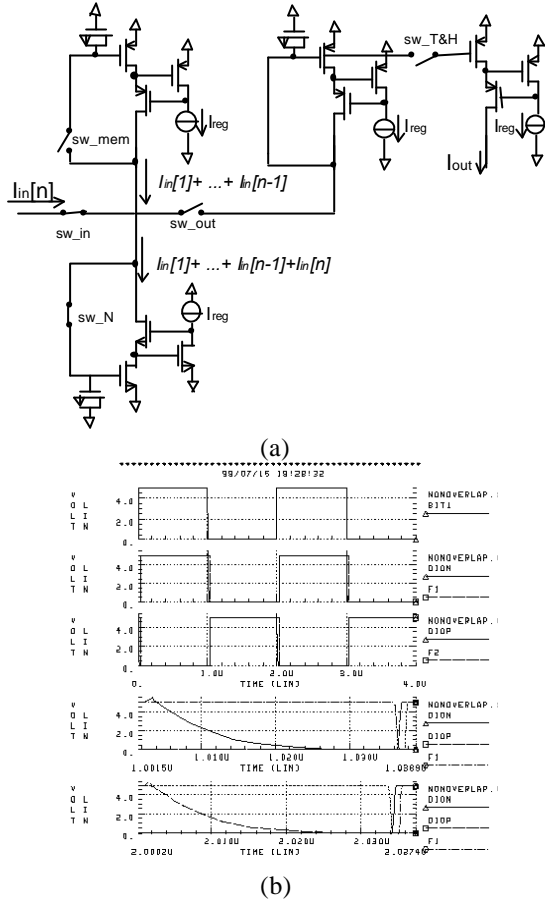
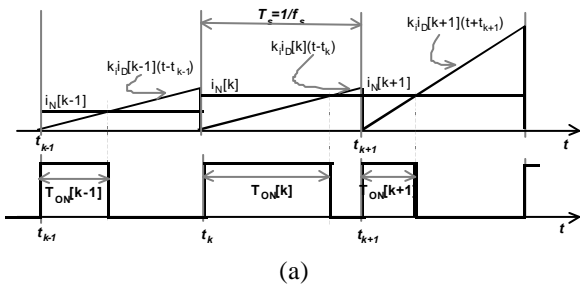
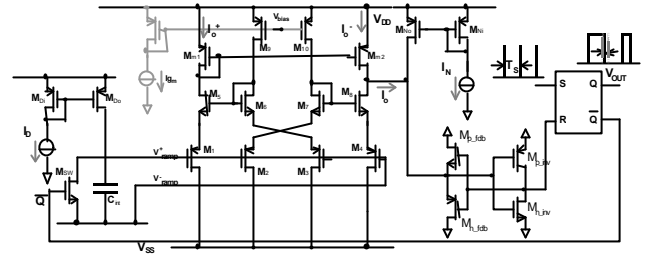


Figure 6. (a) Diagram of the switched-current storing/integrating stage (b) Waveforms of the non-overlapping adjustable-slope clock generator.

As long as the division stage is concerned, it is stressed that, due to the sequential operation of the FKBC, normalization is not allowed, and thus the division operation is required. Its operation is embedded in a PWM stage which drives the output signal.



(a)



(b)

Figure 7. (a) Time diagram of the signals involved in the time-domain division operation. (b) Circuit-level diagram of the current-mode PWM division stage.

Finally, the last stage features the capability of implementing the division operation required by the center-of-area defuzzyfication method, by means of the intrinsic division obtained by a PWM modulator, which is performed by virtue of its signal-to-time conversion. The resulting output signal for the FKBC is, thus, in voltage-mode and PWM modulated. This solution proposed by the authors, is hardware-efficient and appropriate for the fully-integrated fuzzy control of switched power converters, or, in general, any power plant requiring a PWM drive. The circuit is based on the periodic integration of the current associated to the denominator (aggregation of consequent-weighted rule values), thus creating a current-mode ramp signal with its peak level proportional to the signal -fig. 7(a)-. A current-input voltage-output high-speed comparator [15] -fig. 7(b)- compares continuously in time both numerator and denominator accumulated signals, being thus the duty cycle given by:

$$i_N[k] = \frac{g_m}{C_{int}} \int_{t_k}^{t_{k+1}} i_D[k] \cdot dt$$

$$\xrightarrow{t_k \leq t \leq t_{k+1}} i_N[k] = \frac{g_m}{C_{int}} \cdot i_D[k] t$$

$$D_k = \frac{t_{ON}[k]}{T_s} = \frac{C_{int}}{g_m \cdot T_s} \frac{i_N[k]}{i_D[k]} \quad (8)$$

where the division operation appears in an explicit form. The current integration constant is electronically adjustable by varying C_{int} or g_m . C_{int} is an external capacitor outside the integrated circuit, and g_m is the transconductance value of the OTA used to convert voltage-mode integrated signals into current-mode. In order to obtain a wide linear margin, the OTA used in the design is that of Seevinck [17], which exploits the class AB compensation of the nonlinear characteristics of the transistors, as in high slew-rate operational amplifiers [16].

POST-LAYOUT SIMULATION RESULTS

The presented FKBC has been designed and full-custom laid-out using a $0.8\mu\text{m}$ CMOS analogue technology and simulations using extracted circuits show proper operation. As an example, figure 8 shows two performance validation results. Figure 8 (a) shows a

post-layout simulation of the inference block including four membership functions and three MIN operators, programmed sequentially in position and slope but with saw-tooth input signal to show the membership characteristics over the whole input range. On the other hand, figure 8(b) illustrates, with a fully-transistorised sequential-mode simulation, the operation of the FKBC, showing the current-sample accumulation and PWM controller output signal. Figure 9 shows a view of the final layout. The analogue part of this application specific controller features small size –about 0.65mm² for this eight-rule/three-input prototype testchip-, and low power consumption. The fabrication of the testchip is currently in progress.

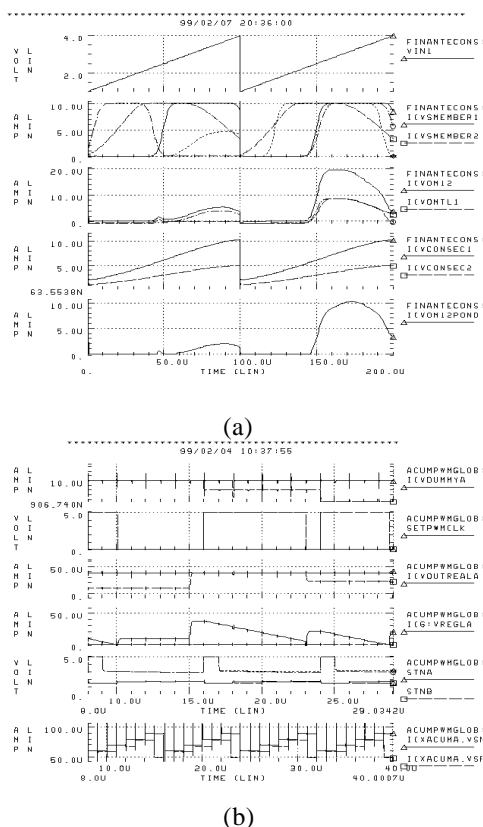


Figure 8. (a) Inference time-domain simulation (b) Discrete-time switched-current integration and PWM output waveforms.

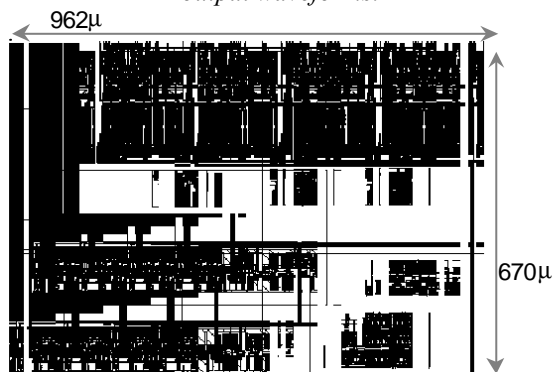


Figure 9. Designed layout for the sequential FKBC. Dimensions shown in μm .

CONCLUSIONS

This communication reported on the design and implementation of a mixed analogue/digital sequential-mode fuzzy controller. Among others cells used in this architecture, the description of the fully adjustable membership function circuit, the voltage/current-mode minimum circuit, current-steering DACs, switched-current analogue memories and PWM division circuits has been presented. Layout-extracted fully-transistorized simulations validate the operation of the FKBC.

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REFERENCES

- [1] T.Takagi and M. Sugeno. "Fuzzy Identification of Systems and its Applications to Modelling and Control". *IEEE Transactions on Systems, Man and Cybernetics*, Vol 15, n°1. January 1985.
- [2] J.R. Jang, "ANFIS: Adapted Network based Fuzzy Inference System". *IEEE Transactions on Systems, Man and Cybernetics*, Vol. 23, n° 3, pp 665-685. May/June 1993.
- [3] M.J. Patyra, J.L. Grantner, K.Koster, "Digital Fuzzy Controller: Design and Implementation", *IEEE Transactions on Fuzzy Systems*, Vol. 4, N°4, November 1996, pp. 439-459.
- [4] S. Guo, L. Peters and H. Surmann, "Design and application of an analog fuzzy logic controller", *IEEE Transactions on Fuzzy Systems*, Vol. 4, N°4, November 1996, pp. 429.
- [5] F. Vidal and A. Rodríguez Vázquez, "Using building blocks to design analog neurofuzzy controllers", *IEEE Micro*, Aug 95, pp.49.
- [6] J.M. Moreno, F. Castillo, J. Cabestany, J. Madrenas and A. Napieralsky, "An analog systolic neural processing architecture", *IEEE Micro*, June 94, pp.51.
- [7] N. Yazdi, M. Ahmadi, G.A. Jullien and M. Shridhar, "Pipelined Analog multiplier feedforward neural networks", *proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS'93)*, pp. 2768.
- [8] J.M. Moreno, J. Madrenas, E. Alarcón and J. Cabestany, "Analog Sequential Architecture for Neuro-Fuzzy Models VLSI Implementation", *Lecture Notes in Computer Science, Artificial Neural Networks-ICANN'97*, Laussane, Oct 1997.
- [9] P. J. Crawley and G.W. Roberts, "Designing Operational transconductance amplifiers for low-voltage operation", *proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS'93)*, pp. 1455.

- [10] K. Bult and H. Wallinga, "A class of analog CMOS circuits based on the square-law characteristic of an MOS transistor in saturation", IEEE Journal of Solid-State Circuits, Vol. 22, N°3, June 1987, pp. 357.
- [11] J. Ramírez-Angulo, K. Treece, P. Andrews, T. Choi, "Current-Mode and Voltage-Mode VLSI Fuzzy Processor architecture", proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS'95), pp. 1156.
- [12] N. Paulino and J.E. Franca, "A CMOS digitally programmable current multiplier", proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS'96), May 1996.
- [13] C. Toumazou, F.J. Lidgey and D. Haigh, Editors "Analogue IC design: The current-mode approach", IEE Peter Peregrinus, London, 1991.
- [14] C. Toumazou, J.B. Hughes and N.C. Battersby, Editors "Switched-Currents: An analogue technique for digital technology", IEE Peter Peregrinus, London, 1994.
- [15] A. Rodríguez Vázquez, R. Domínguez Castro, F. Medeiro and M. Delgado Restituto "High resolution CMOS current comparators: Design and applications to current-mode function generation", Analog Integrated Circuits and Signal Processing, 7, pp-149-165, 1995.
- [16] T. Fiez, H. Yang, C. Yu and D. Allstot, "A Family of High-Swing CMOS Operational Amplifiers", IEEE Journal of Solid-State Circuits, Vol. 24, N°6, Dec 1989.
- [17] E. Seevinck and R. Wassenaar, "A Versatile CMOS linear Transconductor/ Square-Law Function Circuit", IEEE Journal of Solid-State Circuits, Vol. SC22, N°3, June 1987.
- [18] S. Gomáriz, E. Alarcón, J.A. Martínez, A. Poveda, J. Madrenas and F. Guinjoan, "Minimum-time Control of a Buck Converter by means of fuzzy logic approximation", proceedings of The 24th Annual Conference of the IEEE Industrial Electronics Society (IECON'98), Aachen, Aug. 98.
- [19] P. Hasler, C. Diorio, B.A. Minch and C. Mead, "Single Transistor Learning Synapse with Long-Term Storage", proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS'95).
- [20] J. Madrenas, Ivorra, E. Alarcón and J.M. Moreno, 'Injector Design for Optimized Tunelling in Standard CMOS Floating-Gate Analog Memories', proceedings of The 41st IEEE Midwest Symposium on Circuits and Systems (MWSCAS98), Southbend, Indiana, August 1998.