

Integrated Current-Programming Controller for DC-DC Converters using Current-mode Analogue Processing Techniques

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INTEGRATED CURRENT-PROGRAMMING CONTROLLER FOR DC-DC CONVERTERS USING CURRENT-MODE ANALOGUE PROCESSING TECHNIQUES

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ABSTRACT

This paper reports on the design and simulation of a current-programming controller for DC-DC switched power converters. The proposed analogue circuit allows custom integrated circuit (IC) implementation, which apart from a reduction in cost, mass and weight increases reliability. Current-mode VLSI analogue signal processing techniques are considered, resulting in a compact design suitable for high-frequency cycle-by-cycle control. The control circuitry has been laid-out in a standard 0.8 μ m CMOS technology. Post-layout simulation results for this monolithic controller show proper operation at 1Mhz switching frequency.

Key words: Switched DC-DC Converters; Current-programming Control; Monolithic Analogue Controller; CMOS Analogue VLSI; Current-Mode Analogue Design.

1. INTRODUCTION

IN THE development of new control strategies for dc-dc switching regulators, current-mode control constitutes one of the best alternatives to the different techniques used up to now [1]. Current-mode control, or current-programming, as it is often called, is one of the two-loop control methods where an internal high-speed loop provides a pulse-by-pulse control of the switch current or inductor current and an external loop takes care of the voltage regulation. There exist a great number of particular current-mode controllers, as well as significant research work devoted to the modelling and analysis of this class of circuits. All of them emphasize the following benefits of this technique: single-pole transfer function of the open voltage regulating loop; instantaneous and inherent current limiting, ease of paralleling of regulators, and possibility of feedforward of output current and input voltage [2]. Figure 1 illustrates a simplified block diagram of the control

strategy that determines the duty-cycle (D) in the current-mode peak inductor current control. A continuous-time sample of the inductor current signal, a current reference signal (supplied by the outer voltage regulation loop) and a compensating ramp are combined and passed through a comparing stage to provide the pulse-width modulated control signal.

However, modern control strategies for power converters are not straightforward to implement. In this sense, the ASIC technology provides means of efficiently integrating compact, low-cost and low-power controllers [3,4], thus enabling the implementation of such control laws. Additionally, a growing interest is foreseen in fully-integrated, high-speed controllers for the regulation of high-frequency on-chip dc-dc converters sharing the same die as their own loads, and even with switching active devices embedded on the same chip [5,6]. In parallel, there exists the challenge of reducing the number and size of external parts -reactive components-, thus increasing switching frequencies.

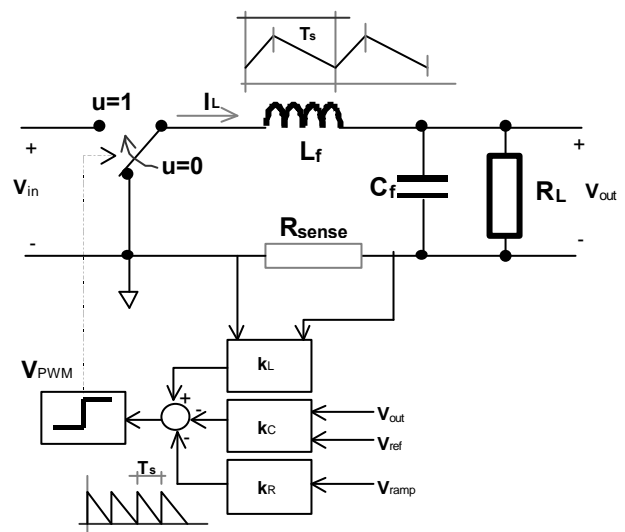


Fig. 1. Buck converter with current-mode control loop.

In order to facilitate integration with other system components, an analogue PWM current-programming controller, compatible with radiation-tolerant technologies [7], has been designed. This analogue PWM modulation is performed in the current-signal domain [8]. In recent years, current-mode circuits [9] have received a considerable attention within analogue VLSI design, mostly because of their attractive characteristics in terms of low-power consumption, small occupied area, compatibility with digital processing circuitry, and high-speed operation capabilities. Current-mode analogue signal processing inherently exhibits wide bandwidth and low-voltage operation, compared with its voltage-mode counterpart. A few successful applications are recently found in the field of power electronics control [10].

In section 2, a detailed description of the adopted circuit configuration is presented. Layout and simulation issues and results are reported in section 3.

2. CIRCUIT DESCRIPTION

The aggregation operation needed at the comparison node of the controller in fig. 1 suggests the use of current-domain representation of signals. In current-mode processing, signal summation is achieved by routing currents delivered by high impedance sources into a single low-impedance node. Regarding the described current-loop controller, current-mode methodology imposes the need to design linear voltage-current converters, current-mode integrators and current-input voltage-output comparators. Design details are discussed in this section.

A. Linear transconductor input stages.

The use of transconductor stages at the input part of the controller provides means of converting external voltages in the power stage to currents within the controller. The transconductors are operated as open-loop voltage-to-current converters, showing high-frequency excellent capabilities but severe requirements in the linear input voltage margin. Several design techniques have been used to extend the linearity range of transconductors, ranging from the use of emitter-degenerating resistors in bipolar technologies [9], its equivalent active source-degeneration in CMOS technologies [11], and several methods exploiting the square-law smooth transconductance characteristics of MOS transistors operated in saturation and strong inversion [9].

The actual design used in the controller exploits the linear, electronically variable, and high bandwidth transconductance of a cell based on two matched MOS

transistors operating in saturation, with the sum of their gate-to-source voltages held fixed. The final linear transconductor block [12] is shown in fig. 2, where floating-bias voltage sources are realized by means of diode-connected CMOS pairs, yielding a cross-coupled differential stage suitable of being operated as a tunable g_m block. This block has been also applied in non-slewing input stages of high-gain high-speed operational amplifiers [13], [14].

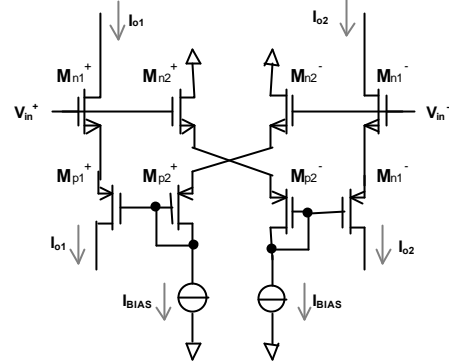


Fig. 2. CMOS Tunable- g_m block.

The transconductance of this block is given by

$$g_m = \frac{I_{o1} - I_{o2}}{V_{in}^+ - V_{in}^-} = \sqrt{8I_{BIAS}} \cdot \frac{b_a}{\sqrt{b_b}} \quad (1)$$

where

$$b_{a,b}^{-1} = (b_{n_{1,2}}^{-\frac{1}{2}} + b_{p_{1,2}}^{-\frac{1}{2}})^2 \quad (2)$$

The linear range is bounded at the input voltage by

$$|V_{in}| < \sqrt{\frac{2}{b_a}} \sqrt{I_{BIAS}} \quad (3)$$

and the constraint in output current is

$$|I_{out}| < |4I_{BIAS}| \quad (4)$$

being the linear current margin more than 100 percent of the total quiescent current.

Regarding second effects, it can be shown that random technology mismatches result in an offset component and a second order distortion term, at the same level as they do in simple two-transistor source-coupled differential pairs. However no matching of n-type and p-type transistors is required. The circuit configuration itself tends to compensate channel-length modulation effect and body effects. For this to be possible, the wells are to be connected to their respective supply voltages, this further reducing parasitic capacitances and enhancing bandwidth limitations.

B. Summation stage.

The previous transconductance cells must be properly loaded to sense their output differential currents by a low-impedance node (nearly constant voltage) while realizing the subtraction operation needed in (1). In the proposed design this is accomplished by means of a folded-cascode summation network. It is pointed out that the combination of several linear V/I stages with an aggregation stage can be viewed as a multiple-input transconductor. Regarding its functionality, this configuration is equivalent to the use of several standalone operational transconductance amplifiers (OTAs) tied together at the output node, but it is optimum as regards to area, power consumption and design complexity.

The folded-cascode subcircuit –shown in transistor-level form in fig. 3–, is composed of two common-gate current buffers and a current mirror at their output. The current that is sourced or drained at the output node corresponds to the addition of the difference of differential input current signals.

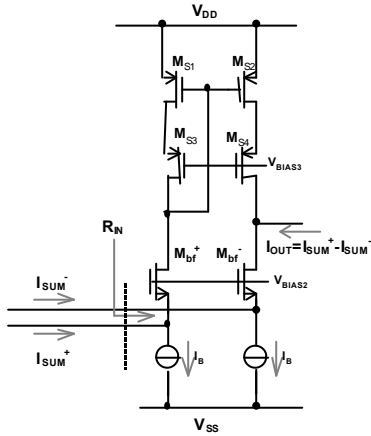


Fig. 3. CMOS Folded Cascode Summation Stage.

An approximate expression for the input resistance at the input node of the folded cascode stage is given by

$$R_{in} \cong \frac{1}{g_m} \left(1 + \frac{R_L}{r_{DS}} \right) \quad (4)$$

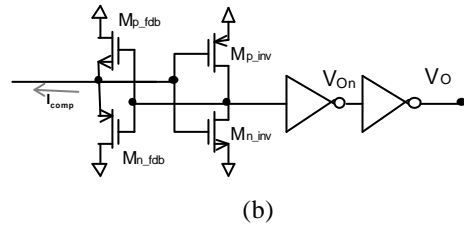
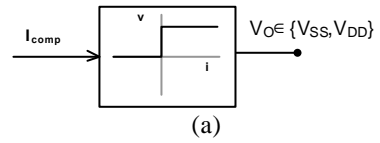
where R_L/r_{DS} stands for the ratio of the load resistance at the output node of common-gate buffers and their output resistance related to the channel-modulation effect. The inverse dependence on the transconductance requires very large aspect ratio transistors biased with moderate currents, to avoid degradation in high-frequency operation.

Finally, the subtraction current mirror has been selected on that of low-voltage, high-compliance cascode current mirror type. This mirror configuration [15] achieves high-accuracy copying and low output conductance by virtue of its cascode operation, while the fact that it avoids a

diode-connected stack prevents a reduction in the output operation voltage margin. The use of cascode stages reduces offset errors at the rule evaluation node.

C. Current Comparator

For a comparator to be load compatible with the previous current summation stage, its input impedance must be low enough to accept positive and negative currents while not changing its voltage level, thus keeping previous stage transistors working in saturation. With this end, a current-input voltage-output comparator is used [16]. The high-level description of its functionality is shown in figure 4(a) and the actual transistor-level circuit is depicted in fig. 4(b). The core of the circuit is constituted by a voltage inverter (M_{n_inv} , M_{p_inv}), which can be interpreted as an analogue amplifier, and a class-AB non-linear voltage-following feedback network (M_{n_fdb} , M_{p_fdb}). This feedback action confers true current-mode operation by reducing the input impedance. Moreover, the circuit operates in continuous-time, with no latch state. In fact, this four-transistor regenerative architecture retains the characteristics of capacitive-input comparators (high precision) and combines the advantage of nonlinear-resistive input to achieve very high-speed operation [17]. Figure 4(c) depicts the delay time dependency on input current level, showing delay values down to 1ns. This circuit has been used previously in analogue-to-digital current-mode conversion architectures, by codifying the sign of the input current in binary form. The capacitive input due to the digital inverter input node results in an integrating action, thus yielding virtually zero current offset. Figure 4(d) illustrates with a transient simulation ($f_{in}=1\text{Mhz}$) its proper behaviour as a current direction detecting circuit and the capability of maintaining a nearly fixed input voltage at half the supply voltage.



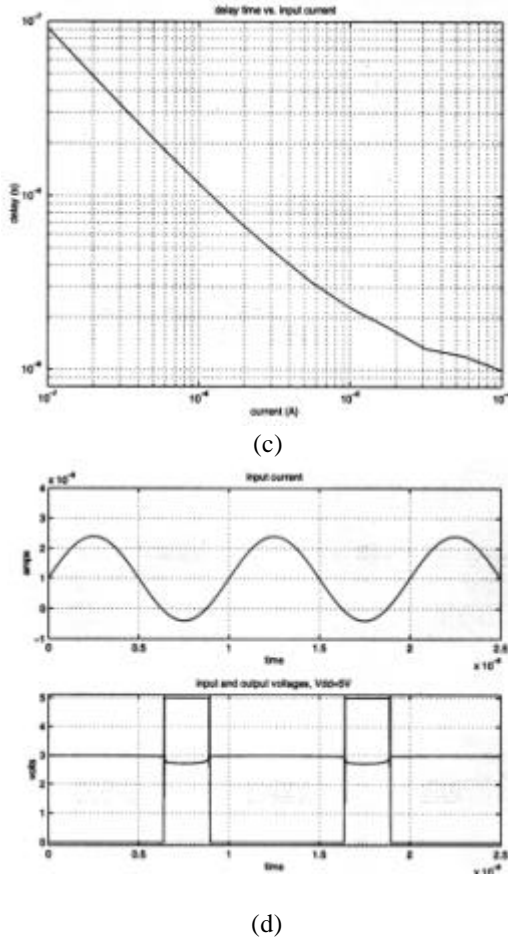


Fig. 4. Transimpedance high-gain comparator: (a) Block-level description (b) Transistor-level circuit implementation (c) Simulated delay versus input current level (d) Simulated transient behaviour.

The output of the comparator is passed through a chain of analogue amplifiers (actually an optimum-sized tapered 4-stage inverter chain to drive the pad loads) so that steeper edge slopes in the output ON/OFF signal are obtained. In fact, the comparator operates by virtue of a transimpedance amplification mechanism, yielding the fastest response for a given technology, which can be exploited to design voltage-mode comparators using one-stage CMOS OTA structures [18].

D. Current Integrator

In order to obtain the linear current compensating ramp required in the controller, pulsed integration has to be performed.

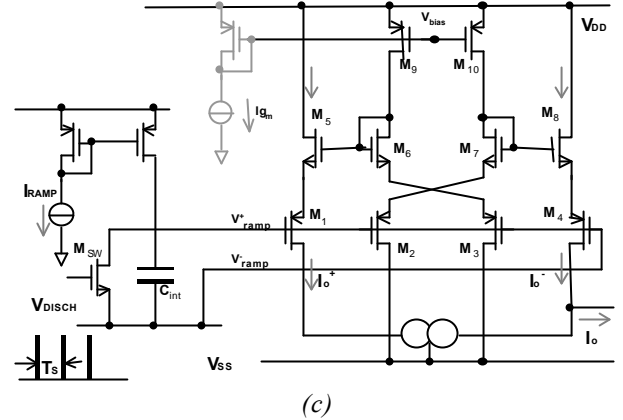
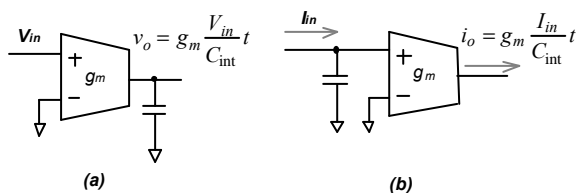


Fig. 5. (a), (b) Open-loop Integrator configurations and (c) transistor-level pulsed-integration description for (b)

Given the availability of capacitive elements in IC domain to perform current integration, voltage integration -fig5(a)- or current integration -fig5(b)- is obtained by shifting the circuit configuration of a capacitor and a transconductor. Both open-loop configurations are optimum, as long as speed is concerned, compared to their opamp-based close-loop equivalents. Hence, current-input current-output pulsed integration is finally obtained by the circuit depicted in fig. 5(c), which consists of a current-mirror acting as a current buffer and sourcing input-dependent current to the capacitive node. Being this capacitor periodically switched by transistor M_{SW} at a rate T_s , the output current of the transconductor consists of a sawtooth current signal. The common-mode input voltage range of the transconductor captures ground potentials by the use of p-channel input devices. This transconductor structure is the complementary version of that in fig. 2.

At high operation frequencies the issue of clock feedthrough must be addressed at the design stage. ON-to-OFF transients result in a negative charge injection from the pulse signal to the integrating node via the switch transistor's gate-to-drain overlap capacitance. Analytically,

$$e_{voltage} = \frac{C_{ov}}{C_{INT}} \cdot (V_{HIGH} - V_T) \cdot a C_{ov} \cdot a W_{SW} \quad (6)$$

which illustrates the dependence of the voltage error on the width of the switch transistor.

In addition to the charge injection phenomena, and in order to ensure capacitor discharge, a variable short-pulse generator has been included in the design. This block, not fully described here, is composed of a one-side starved inverter [4] and a XOR logic gate to obtain, from an external clock signal, a pulse train with externally adjustable width (t_{DISCH}). Switch transistor's aspect ratio is to be high enough to satisfy:

$$t_{DISCH} > n R_{ON_{sw}} C_{INT} \cdot a \frac{C_{INT}}{k' (W/L) V_{OV}} \quad (7)$$

while not compromising the charge injection effect –eq. (6)–, for a given integrating capacitance value.

3.SIMULATION RESULTS OF PROTOTYPE CONTROLLER

The presented current-mode controller was designed and laid-out using a 0.8 μ m CMOS double-poly double-metal technology, and simulations using parasitics-extracted circuits show proper operation. To test and evaluate the behaviour of the controller, a buck DC-DC converter plant with ideal switches, $L_f=175\mu\text{H}$, $C_f=0.22\mu\text{F}$ output filter and $R_L=5\Omega$, $R_{\text{SENSE}}=0.8\Omega$, $V_g=5\text{V}$ and $i_{L,\text{ref}}=0.4\text{A}$ was considered. The switching frequency was set up to 1MHz in order to stress the high-frequency capability of the current-mode design approach. The complete diagram of the controller is shown in figure 7 with its related transistor sizes. Each transconductance block has external independent control of its g_m value, to increase flexibility, and so, the equation that models the state change is given by:

$$g_{m_1}V_C + (-g_{m_2} \frac{i_{\text{RAMP}}}{C_{\text{int}}}) = g_{m_3}R_{\text{SENSE}}\dot{I}_L \quad (8)$$

As an example of operation, figure 6 shows two performance validation results. Figure 6(a) shows, with a post-layout full-transistor HSPICE® simulation, the action of the current-programming law. Specifically, the upper graph shows the time-domain evolution of the monitored inductor current, command current and current compensating ramp. The second and third traces show the waveforms of the comparator input current and the PWM output voltage associated to its change in direction (zero-crossings). Notice the fast edges of the time-modulated ON-OFF signal. Bottom traces correspond to other signals relevant for the controller, the voltage at the integrating node of the compensating ramp and at the current-sensing resistor, and superimposed, the inductor current. An enlargement of the upper traces in fig 6(a) is represented in fig 6(b), where it is apparent that the off-switching instant is forced by the crossing of inductor-current sample-current with the command and the ramp compensating currents. At 1Mhz constant switching frequency, no delay time is appreciated in this cycle-by-cycle control, albeit signal levels are well below 10 μ A -i.e. low-power consumption-. Other results include Monte Carlo simulation, in order to account for IC mismatch effect, which showed 100% yield (out of 15 trials). For illustration purposes, figure 8 corresponds to the layout of the full controller, where biasing circuitry is omitted. Guard rings are used as a layout strategy to avoid coupling in this mixed-signal environment, as well as latch-up. The actual dedicated controller features small size –about 0.028mm²–, and low power consumption.

CONCLUSIONS

This paper reported on the design and simulation test of an analogue controller IC for switched DC-DC power converters, intended to provide current-mode peak inductor current control. The use of modern current-mode analogue signal processing techniques results in high-frequency low-power operation in a standard 0.8 μ m CMOS technology, being thus compatible and allowing potential use with on-chip loads, on-chip power switching devices or even reactive components within a complete smart power chip. The fabrication of the controller is in progress.

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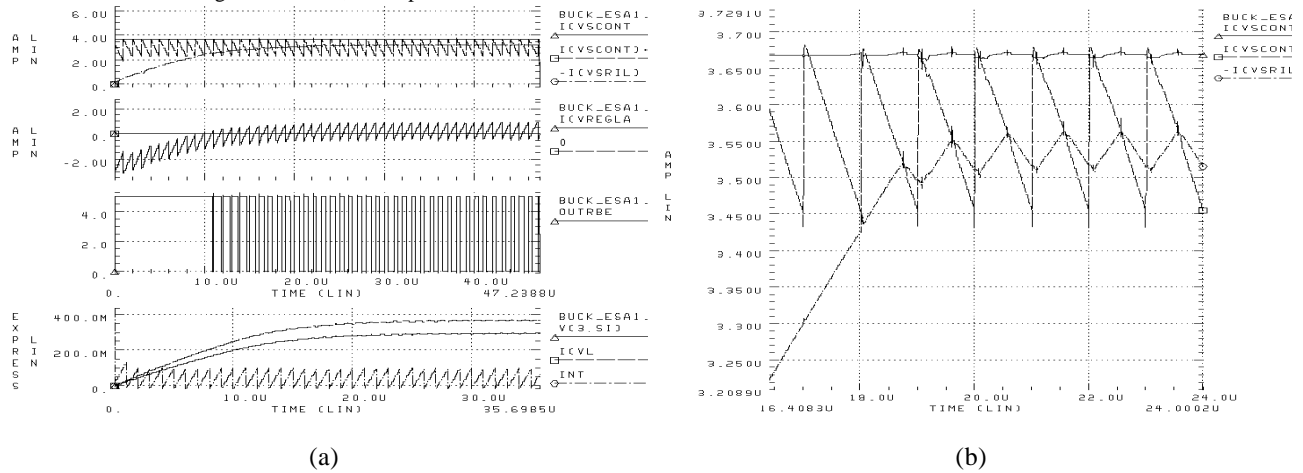
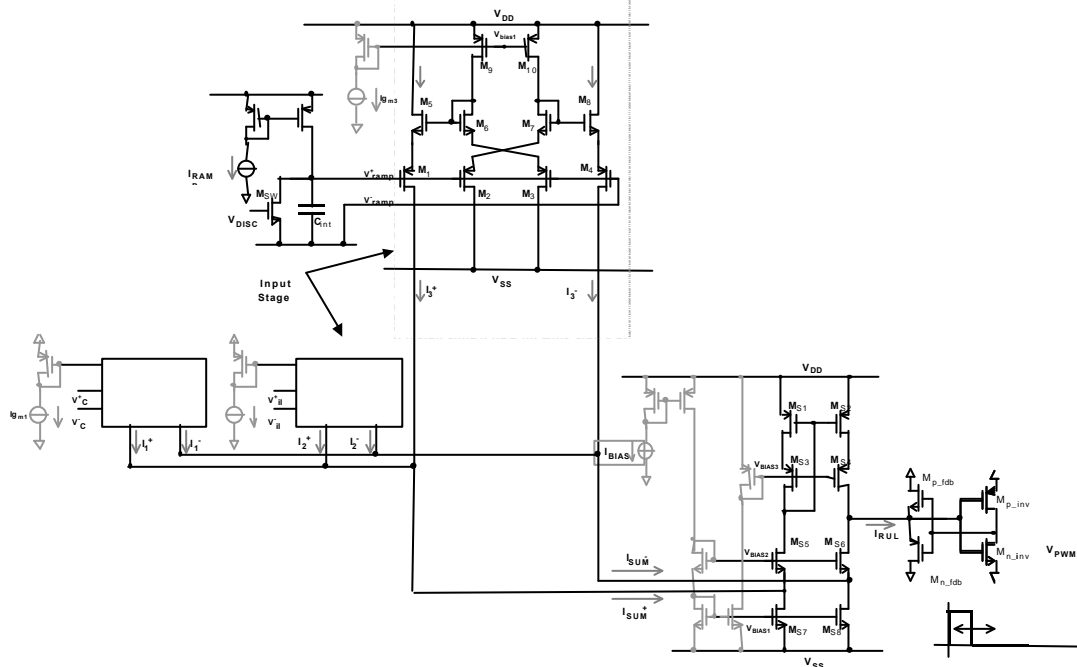


Figure 6. Simulation results . See text for details.



	M _{S1-6}	M _{S7,8}	M _{D fdb,} n inv	M _{D fdb,} n inv	M _{SW}	M ₁	M ₂	M ₃	M ₄	M ₅	M ₆	M ₇	M ₈
(W/L)	50μ/0.8μ	50μ/0.8μ	2μ/0.8μ	5μ/0.8μ	10μ/0.8μ	20μ/0.8μ	17μ/0.8μ	17μ/0.8μ	20μ/0.8μ	10μ/0.8μ	8μ/0.8μ	8μ/0.8μ	10μ/0.8μ

Figure 7. (a) Diagram of proposed VLSI current-mode controller. Transistor Sizes.

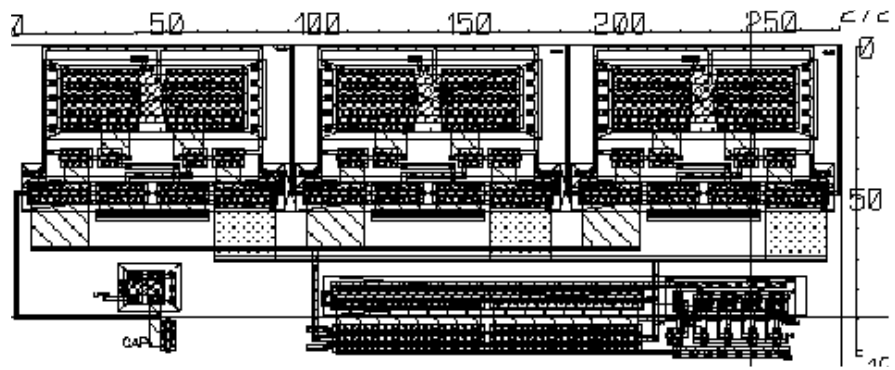


Figure 8. Sample layout of the controller in a 0.8 μm standard CMOS technology.