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# Noise and Speed Performance in Switched-Current Memory Cells\*

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**Abstract** - In this paper, speed and noise issues are reviewed in switched-current memory cells, concerning the copying accuracy. Optimum criteria for added storing capacitors and design parameters are derived for both speed and noise, as a function of clock frequency. A merit factor is defined including both factors and is analytically shown to be dependent on the area of the copy transistor. AMS-0.8 $\mu$ m process HSPICE simulation results validate these analysis.

## I. INTRODUCTION

THE current copier or switched-current memory cell is the basic building block in switched-current analogue signal processing. Its operation is intended to avoid mismatching errors, and it is based on dynamic sampled-data analogue techniques leading to theoretically error-free current-sample copying capabilities. In addition to this, the current copier can be implemented in single-poly digital CMOS VLSI technology, and this justifies the considerable efforts and advances in this area. The switched-current technique has been successfully applied [1] to the design of digitally programmable switched-current filters, ratio-independent multipliers/dividers, self-calibrating D/A converters and sigma-delta front ends. The analogue storing capability of the current copier has also been proven to be useful in the design of mixed-signal systolic neural processor implementations [2].

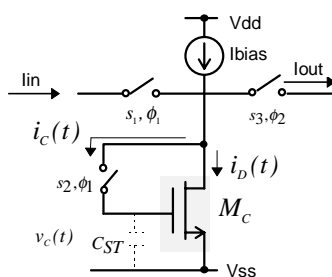


Figure 1. Basic Current Copier Cell.

In practice, however, there are several non-idealities limiting the current copier performance [3]. The basic current memory cell is depicted in figure 1. During clock phase  $\phi_1$ , MOS switches  $s_1$  and  $s_2$  are closed and, thus, the diode-connected copying transistor develops a gate voltage corresponding to the input current (through the square-law relationship). During the second phase  $\phi_2$ , switches  $s_1$

and  $s_2$  are left open, while MOS switch  $s_3$  connects the copy transistor drain to the output load. Since the storing gate capacitor  $-C_{ST}$  (due to the intrinsic gate-to-source capacitance or an explicitly added capacitor) stores the analog information in voltage form, and, provided the copy transistor remains saturated, the output current ideally equals that of the input current in phase  $\phi_1$ .

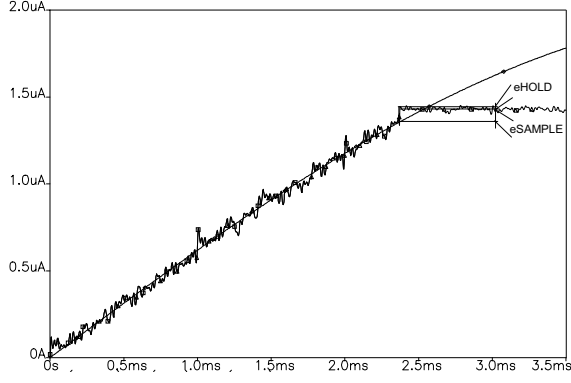
From this operation mechanism, several error sources affecting the current copier performance (actually, the copying accuracy) are expected. Namely, charge-injection and clockfeedthrough effects, non-zero output conductance, and finite speed -i.e. settling time-, result in a copy error. Furthermore, a certain non-deterministic error arises due to copier transistors noise. Many circuitual techniques have been proposed to reduce the first two effects. On the one hand, the use of regulated cascoding techniques improves the output impedance level so as to neglect its effect. On the other, in order to reduce errors due to charge injection, complementary CMOS transmission gates with dummy switches may be used. The use of more complex clocking schemes (i.e., S<sup>n</sup>I technique) proves also useful to reduce clockfeedthrough effects. Nevertheless, the circuit-level reduction of these previous effects leaves fundamental effects -speed and noise- as actual limitations.

The scope of this paper is to review noise and speed/settling-time topics for non-periodically switched copiers (memory cells) and to obtain some guides for designing device sizes and bias ( $W, L, I_{bias}$ ) as long as eventually added storing capacitances.

## II. NOISE ANALYSIS

In this section the current copier noise will be characterized as an effect which limits the maximum achievable resolution -in equivalent bits- during the storing process. Figure 2 shows the time-domain sampling-and-hold process.

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**Figure 2.** Time-domain noise sampling process.

When the input current to the memory cell is of value  $i_{in}$ , the output value results in

$$i_o = i_{in} + \Delta i_{n\ sample} + i_n(t)_{hold} \quad (2.1)$$

where the second term is a non-deterministic constant offset due to sampled noise, and the third term is a time-dependent noise component. The former's level is related to the copy transistor bandwidth, while the variant component is related to the load stage bandwidth.

In principle, both copying and switch transistors contribute to the noise at the storing capacitor. However, in the actual circuit, and owing to the feedback connection, the noise introduced by the switch is negligible as shown in (2.2), where  $S_x^y(f)$  represents the mean-square noise voltage density.

$$S_{V_c M_{sw}}^S(f) = \frac{\left(\frac{g_o}{g_m}\right)^2}{1 + \left(\frac{f}{f_o}\right)^2} S_{M_{sw}}(f) \xrightarrow{\frac{g_o}{g_m} \ll 1} \approx 0 \quad (2.2)$$

The spectral noise density due to the main transistor is filtered by the loop's bandwidth  $-f_o-$  (2.3). This spectral density consists of both flicker (1/f) and white noise components (2.4).

$$S_{V_c M_c}(f) = \frac{1}{1 + \left(\frac{f}{f_o}\right)^2} S_{M_c}(f) \quad (2.3)$$

$$S_{V_c M}^S(f) = \frac{4kT}{3g_m} + \frac{KF_n}{C_{OX}WL} \cdot \frac{1}{|f|} \quad (2.4)$$

If the current copier is periodically switched, the noise components -white and 1/f- are also periodically sampled and held; thus, the spectral noise density is repeated at harmonics of the switching frequency, and the hold time effect is the familiar sinc-shaped spectral conformation. Analytically,

$$S_i^{S/H}(f) = g_m^2 S_{V_c}^{S/H}(f) = g_m^2 \text{sinc}^2(f \cdot T_{hold}) \cdot \sum_{n=-\infty}^{n=+\infty} S_{M_{IC1}}(f - n f_s) \quad (2.5)$$

However, if the current copier is intended to work as a memory cell ( $f_s \rightarrow 0$ ), only the time interval  $nT_s < t < (n+1)T_s$  has to be considered, and, thus, only the baseband noise holds (2.6):

$$S_{i_D}^S(f) = g_m^2 S_{V_c M}^S(f) \quad (2.6)$$

As long as the variant component in the hold phase is concerned, the same expression (2.3) applies if the load bandwidth is considered, without loss of generality, to be the same as the cell bandwidth, which is a reasonable assumption if the memory cell is loaded with another current copier.

Finally, in order to establish a criterion for noise level characterization from the accuracy of the current copier point of view, an expected value of current  $\sigma_{ni}$  is obtained integrating the spectral density (2.6) over the cell's own bandwidth.

$$\begin{aligned} \bar{i}_{TOT}^2 &= \int_0^{\infty} S_{TOT}(f) df = \\ &= \int_0^{\infty} S_{i_D}^S(f) + S_{i_D}^H(f) df = \\ &= 2 \int_0^{\infty} S_{i_D}^S(f) df = \\ &= 2 \int_0^{\infty} g_m^2 \frac{1}{1 + \left(\frac{f}{f_o}\right)^2} \cdot \frac{4kT}{3g_m} \cdot df = 2g_m^2 \cdot \frac{4kT}{3g_m} \cdot \frac{g_m}{4C_{ST}} \end{aligned} \quad (2.7)$$

In the previous expression (2.7), the approximation of ignoring flicker noise has been made, this yielding simpler expressions. This assumption is valid since the relative value of 1/f noise is lower than 1% of the white noise for typical bandwidth values. This noise power includes both sampled noise (constant copying error) and direct noise (time-variant output error). Accordingly, its square root represents the expected current noise at the cell's output (2.8):

$$\sigma_{ni} = \sqrt{\bar{i}_{TOT}^2} = g_m \sqrt{\frac{2kT}{3C_{ST}}} \quad (2.8)$$

This value, which depends on design parameters (through  $g_m$  and  $C_{GS}$ , and their dependence on  $I_{BIAS}$ ,  $W$  and  $L$ ), will be considered as a measure of the copying error due to noise.

### III. SPEED/SETTLING-TIME CONSIDERATIONS

The current copier operation bandwidth can be defined as the frequency margin of clock rate over which the error due to either high-frequency or low-frequency dynamics become greater than the equivalent bit resolution.

Regarding low frequency effects, the error bound is imposed by the discharge of the storing capacitor, through the reverse-biased junction of the turned-off switch transistor. In order to minimize this effect, the ratio between the storing capacitor and the switch transistor dimensions must be increased which, in turn, reduces clockfeedthrough effect.

The high-frequency effect bound is observed in the time domain as a non-negligible settling time which limits the accuracy. In non-periodically clocked memory cells, the design procedure is to obtain the size of the storing capacitor, bounding the settling time caused error -for a certain sample time- and to infer the storing time over which the cells holds the memorized value within the required resolution.

Considering the settling time issue, a reasonable model is that the memory cell response is that of a first-order settling due to a real pole -loop bandwidth-, after

$$\omega_o = 1/\tau = \frac{g_m}{C_{ST}} \quad (3.1)$$

In order to properly use this model, the issues of nonlinear settling and second-order dynamics are treated in next sections, obtaining the working conditions to assure the operation stated in (3.1).

#### A. Nonlinear Settling.

A first order small-signal linearized model for the circuit topology of figure 1, in the sampling phase, yields

$$i_D(t) = i_1 + \Delta i (1 - e^{-t/\tau}) \quad (3.2)$$

However, in actual current copier applications working as memory cells, the input current is expected to vary widely. As a consequence, the linear model which yields (3.2) is no longer valid, and an analysis including the square-law relation between gate voltage and drain current must be used when solving the nonlinear differential equation -figure 3-.

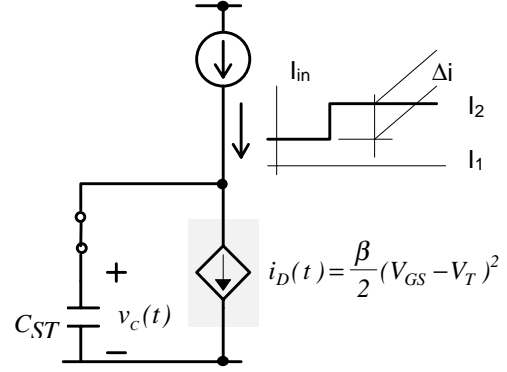


Figure 3. Nonlinear settling circuit model.

This analysis yields a nonlinear settling for the copying transistor drain current as [4],

$$I_D(t) = I_2 \left( \frac{\sqrt{I_1 + \sqrt{I_2}} + (\sqrt{I_1} - \sqrt{I_2}) e^{-\frac{\sqrt{2I_2}\beta t}{C_{ST}}}}{\sqrt{I_1 + \sqrt{I_2}} - (\sqrt{I_1} - \sqrt{I_2}) e^{-\frac{\sqrt{2I_2}\beta t}{C_{ST}}}} \right)^2 \quad (3.3)$$

After the SPICE simulation in figure 4, it can be concluded that the shape of the waveform is not critical. In this simulation there are superimposed the responses due to linearized models with transconductances of maximum and minimum values, and the inner curve is that of the actual device (nonlinear).

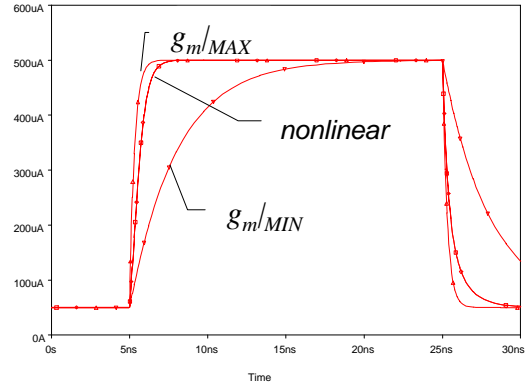
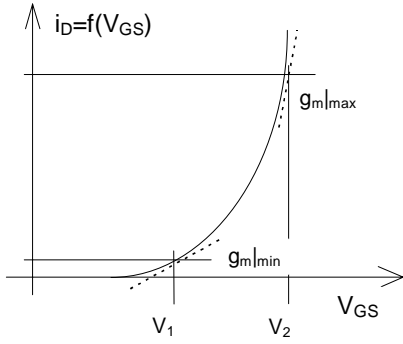


Figure 4. Linear/nonlinear settling comparison.

Qualitatively, the equivalent linear transconductance for the nonlinear settling in a first-order model will be somewhere between the minimum and maximum transconductance values as indicated in (3.4) and in figure 5.

$$g_{mMIN}(I_1) \leq g_{mEQ} \leq g_{mMIN}(I_2) \quad (3.4)$$



**Figure 5.** Nonlinear settling circuit model.

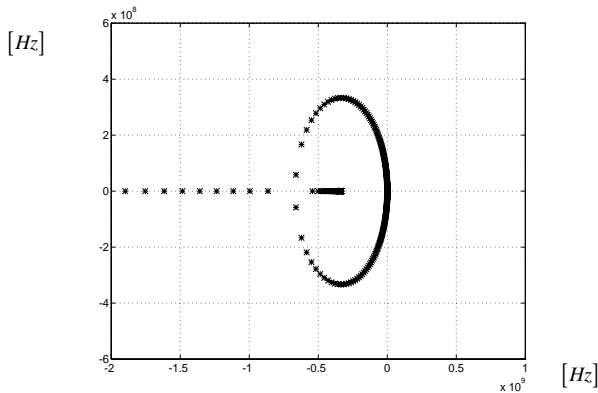
### B. Second Order Settling.

When the linearized version of the circuit in figure 1 is extended including parasitics such as switch ON resistance ( $r_s=1/g_s$ ) and load capacitance ( $C_{OUT}$ ), the transfer function between input current and drain current becomes

$$H(s) = \frac{i_D(s)}{i_{IN}(s)} = \frac{I}{I + s \left( \frac{C_{ST} + C_{OUT}}{g_m} \right) + s^2 \left( \frac{C_{ST} C_{OUT}}{g_m g_s} \right)} \quad (3.5)$$

One way of analyzing qualitatively the effect of switch resistance over the dynamic response of the cell is to represent the root locus -figure 6- of the poles in (3.5) considering the switch resistance  $r_s$  as a parameter:

$$\begin{aligned} I + s \left( \frac{C_{ST} + C_{OUT}}{g_m} \right) + s^2 \left( \frac{C_{ST} C_{OUT}}{g_m g_s} \right) &= 0 \Rightarrow \\ s^2 \left( \frac{C_{ST} C_{OUT}}{g_m} \right) & \\ \Leftrightarrow I + r_s \frac{s^2 \left( \frac{C_{ST} C_{OUT}}{g_m} \right)}{I + s \left( \frac{C_{ST} + C_{OUT}}{g_m} \right)} &= 0 \end{aligned} \quad (3.6)$$



**Figure 6.** Loop gain Root Locus as a function of  $r_s$ .

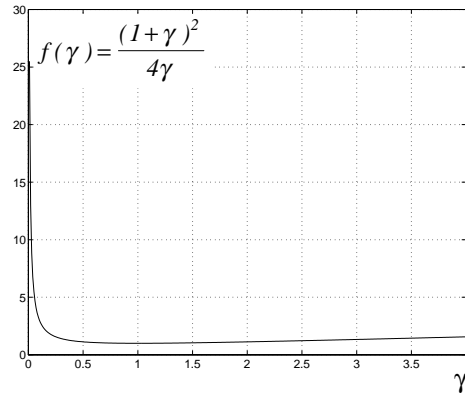
As it can be extracted from this pole locus, considering zero switch resistance leads to a pure first-order settling behavior -with the time constant as

defined in (3.1)-. When increasing  $r_s$ , the cell responds more rapidly and reaches a minimum settling time (about half the intrinsic time constant), for a  $r_s$  value  $-r_{scrit}$  just before the poles become complex and overshooting occurs. After this  $r_{scrit}$  value, the cell slows down, since the poles' real part - which is related to the envelope settling time- is lower. The value of the maximum speed resistance  $r_{scrit}$  can be derived from the quality factor of the second order denominator in (3.4), which is

$$Q = \frac{\sqrt{\frac{g_m}{g_s} C_{ST} C_{OUT}}}{C_{ST} + C_{OUT}} \xrightarrow{C_{OUT} = \gamma C_{ST}} Q = \frac{\sqrt{\frac{g_m}{g_s} \gamma}}{1 + \gamma} \quad (3.7)$$

In this definition, a certain load capacitance  $C_{OUT} = \gamma C_{ST}$  has been considered. When the quality factor is 0.5,  $r_s$  corresponds to the maximum cell's speed.

$$Q = 0.5 \Rightarrow r_{scrit} = \frac{1}{g_m} \cdot \left[ \frac{(1 + \gamma)^2}{4\gamma} \right] \geq \frac{1}{g_m} \quad (3.8)$$



**Figure 7.**  $r_{scrit}$  dependence on load capacitance.

In figure 7, it is depicted the factor which depends on the load capacitance and it can be observed that for  $\gamma > 0.5$ , the critical switch conductance is in the order of the transconductance. This is again a nonlinear phenomenon, since the linear response of the cell (speed and overshoot amount) depends on the input current level through  $g_m$ .

Concerning settling behavior, it can be concluded that the valid response model of the cell is that of first-order dynamic settling (3.1). Indeed, the copying error due the settling time can always be bounded by a first order exponential decay.

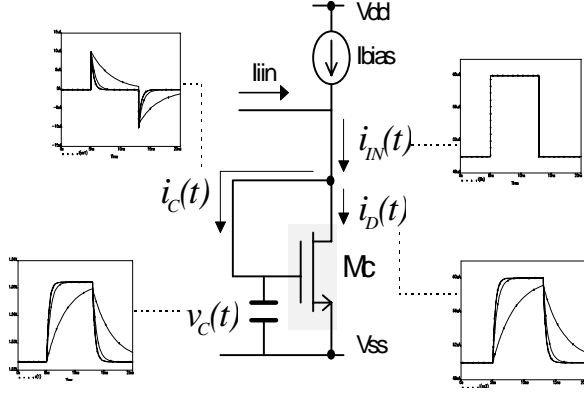


Figure 8. Charging process.

From figure 8 time-domain representation of the storing capacitor charging process, it can be deduced that the current error which limits the resolution is the difference between the input value and the drain current at the end of sample time, which, in turn, is the current flowing to the capacitor.

$$\Delta i(1 - e^{-t/\tau}) = \Delta i - \epsilon_{ST} \quad (3.9)$$

#### IV. OPTIMUM CONDITION

The main scope of this work is to establish some design criteria for speed and noise performance in the current copier-based memory cell.

One approach is to compensate, with an added gate capacitance, the cell bandwidth so as to reduce the output noise. Obviously this compensation depends on the clock frequency. For low input clock frequencies, the noise reduces the maximum achievable resolution. This compensation, however, slows down the speed. In order to solve this trade-off, the sum of both errors must be minimized. The error due to settling time, in relation with added capacitance  $-C_{ADD}$ - and the sample time, follows the expression:

$$\epsilon_{ST} = \Delta i e^{-t/\tau} \xrightarrow{t=T_S} \Delta i e^{-T_S/\tau} \quad (4.1)$$

$$\tau = \frac{C_{ADD} + C_{GS}}{g_m} \rightarrow \Delta i e^{-\frac{T_S g_m}{C_{ADD} + C_{GS}}}$$

Note that  $C_{ADD}$  can be, in general, nonlinear; it is usually implemented with a drain-source shorted transistor. The error due to noise depends only on total storing capacitance ( $C_{GS} + C_{ADD}$ ), after:

$$\epsilon_{NOISE} = \sqrt{i_{NOISE}^2} = \sqrt{i_{NOISE}^2}_{SAMPLE} + \sqrt{i_{NOISE}^2}_{HO} \quad (4.2)$$

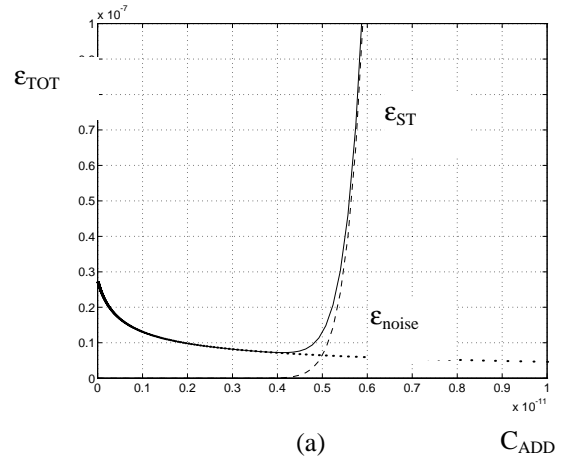
$$= g_m \sqrt{\frac{2}{3} \frac{kT}{C_{ADD} + C_{GS}}}$$

Maximum resolution is obtained when the total error (4.3) is minimum:

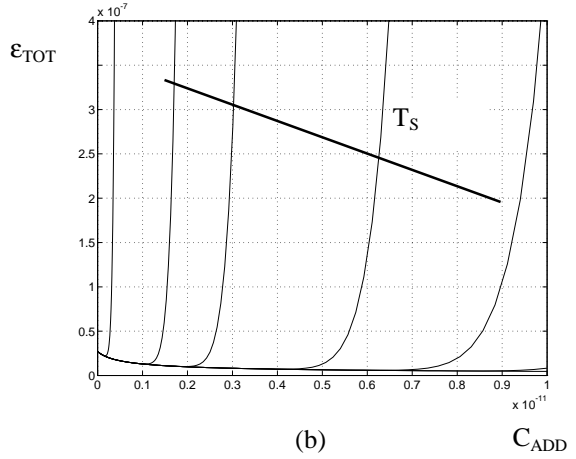
$$\epsilon_{TOTAL}(C_{ADD}, T_S) = \epsilon_{ST} + \epsilon_{NOISE} = \quad (4.3)$$

$$= \Delta i e^{-\frac{T_S g_m}{C_{ADD} + C_{GS}}} + g_m \sqrt{\frac{2}{3} \frac{kT}{C_{ADD} + C_{GS}}} \leq \frac{I_{MAX}}{2^b}$$

Figure 9(a) depicts expressions (4.1), (4.2) and (4.3), varying the added capacitance. From figure 9(b), it can be observed that the compensation capacitor increases when increasing sampling time  $-T_S$ -, and that the total error is further reduced.



(a)



(b)

Figure 9. Minimum error for different added capacitances.

One practical aspect is that the actual compensation capacitor must be less than the obtained value, since, if process variations occur so that the capacitance is greater than expected, the error rises exponentially, worsening the non-compensated cell response.

Finally, another, more general approach, is to optimize a merit factor defined, without considering added capacitors, as the quotient of intrinsic bandwidth over noise, as a function of design parameters, namely:  $W, L$  and bias current. Both

bandwidth and noise dependence is derived from previously stated approximations (2.8) and (3.1) as:

$$BW \cong \frac{I}{\tau} = \frac{g_m}{C_{GS}} \alpha \frac{\sqrt{I_{BIAS}} \sqrt{\frac{W}{L}}}{WL} \longrightarrow \alpha \begin{cases} I_{BIAS}^{1/2} \\ W^{-1/2} \\ L^{-3/2} \end{cases} \quad (4.4)$$

$$\sqrt{i_s^2} \cong g_m \sqrt{\frac{2kT}{3C_{GS}}} \alpha \frac{\sqrt{I_{BIAS} \cdot \frac{W}{L}}}{\sqrt{WL}} \longrightarrow \alpha \begin{cases} I_{BIAS}^{1/2} \\ L^{-1/2} \end{cases} \quad (4.5)$$

Accordingly, the relation of the merit factor  $\eta$  to the design parameters is:

$$\eta(I_{BIAS}, W, L) = \frac{BW(I_{BIAS}, W, L)}{\sqrt{i_s^2}(I_{BIAS}, W, L)} \Rightarrow \alpha \frac{I}{\sqrt{WL}} \quad (4.6)$$

This equation states that this merit factor is independent on bias current and increases when reducing copy transistor area. This result is validated through simulation results of a 0.8um AMS process - figure 10- .

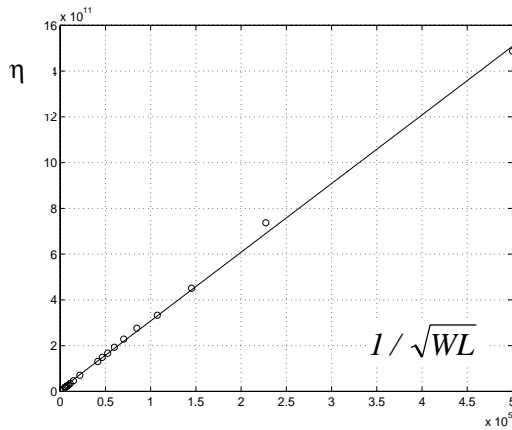


Figure 10.  $\eta(I_{BIAS}, W, L)$  simulation results.

## V. DISCUSSION

One concluding remark is that equation (4.6), which relates the merit factor to design parameters, also applies to continuous-time current mirrors. However, in these circuits, mismatching follows the same dependence over transistor area [5] and, thus, transistors must be designed large enough to assure a certain matching degree. In current copiers, matching is assured by their own switching nature where the same transistor is time-shared, and therefore, transistors can be designed to maximize speed and minimize noise according to (4.6).

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