

HIGH-FREQUENCY RESPONSE MODELLING OF CONTINUOUS-TIME CURRENT MIRRORS

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Abstract — A general analytical model for the frequency-domain behaviour of current mirrors is presented. The proposed model accounts for high frequency effects. The validity of the model it is shown not to be technology dependent. In addition to this, a circuit-level model of the response is derived. The inclusion of this model into high-speed amplifiers macromodels proves useful when predicting phase margins.

I. INTRODUCTION

THE current mirror is well-known for being an ubiquitous building block in analog signal processing circuits, either in discrete or integrated versions. It is used in current-mode analog-to-digital and digital-to-analog data converters, in VLSI implementations of analog or mixed-signal artificial neural networks [1] and also in amplifier design. In this last application, where current mirrors are used as active loads or as supply-current sensing circuits, there is a need for accurate frequency modelling of the mirrors. The reason is that current mirror excellent high frequency behaviour becomes second-order dynamics in amplifiers [2], thus affecting stability in closed-loop configurations. In addition to this, higher order current mirror dynamics can be important in continuous-time integrated current-mode filters [3].

Several current mirrors' characteristics have been previously studied, mainly low frequency effects [4], such as maximum output swing, output impedance, and copying accuracy -which is related to transistors' mismatch in CMOS technologies, and base currents in bipolar technologies-. Previous works propose different transfer functions in the frequency domain for each type of current mirror and technology [5], thus being difficult to shift from one model to other. In this paper a general behavioural frequency model is presented which is valid for each technology (bipolar or CMOS) and can be adjusted for every type of mirror.

In section II the proposed model is introduced, starting with a CMOS simple current mirror analysis, following with a discussion of the validity of the model for small-sized transistors, an extension to bipolar technology and finally, the application of the model to advanced mirror

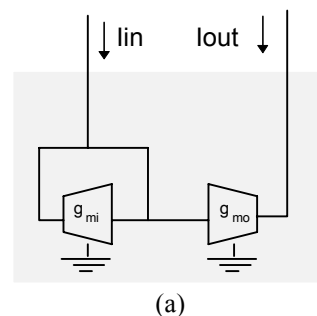
designs. Section III introduces a circuit-level model suitable for the proposed analytical model and for its inclusion in amplifiers macromodels. Finally, the model is used in section IV to accurately predict the phase margin of a current feedback amplifier.

II. FREQUENCY RESPONSE MODELLING

In this section a high-frequency model for a MOS two-transistor mirror is extracted, using small-signal technology-related parameters. This model, when generalised, will be shown to be valid for any type of mirror, and more useful when the size of transistors is reduced. The model can be also applied to bipolar or BiCMOS implementations and also other designs such as high-speed compensated mirrors.

A. MOST current mirror analysis

Figure 1(a) shows a general conceptual model for a current mirror, which is described by two transconductors, connected so as to obtain low input impedance and high output impedance, providing current buffering. The basic version based on transistors is shown in fig. 1(b). It is composed of a drain-gate connected (diode) transistor, which develops a gate-source voltage (V_{gs}) due to the input current, and a transistor acting as a VCCS which is driven by this voltage and hence copies the input current at the output node.



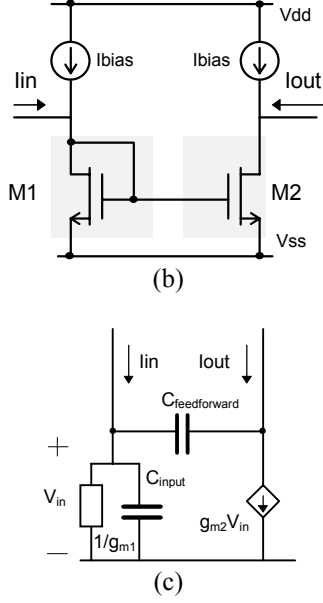


Figure 1. (a) General current mirror model, (b) transistor-level simple mirror schematic and (c) small-signal model

If the transistors are assumed to operate in their saturation regions, the simple current mirror first-order model exhibits a single real pole formed by the small-signal transconductance of the input transistor (M_1) and the capacitance associated to the internal node, actually the sum of both transistors gate-source capacitance (1). It is also shown the relation of the pole to design parameters, namely, bias current and transistor shape.

$$\left. \begin{aligned} g_{m1} &= \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right)_1 I_{bias}} \\ C_{gs} &= \frac{2}{3} C_{ox} WL \end{aligned} \right\} \Rightarrow \omega_p \cong \frac{g_{m1}}{2C_{gs}} = \frac{\omega_T}{2} \alpha I_{bias}^{1/2} \cdot W^{-1/2} \cdot L^{-3/2} \quad (1)$$

However, a complete small-signal analysis yields a transfer function which is characterised by a real pole (the aforementioned one) and a higher frequency right half-plane (RHP) real zero, given by

$$H_{cm}(s) \cong \frac{1 - \frac{s}{\omega_z} C_{dg}}{1 + 2 \frac{s}{\omega_p} C_{gs}} = \frac{1 - \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}} \quad (2)$$

Without loss of generality, a unity-gain current mirror has been assumed. The trade-off between gain and bandwidth in current mirrors has been treated elsewhere [6]. This 1-pole 1-zero frequency response model can be easily interpreted, since it is closely related to physical capacitances. As it is shown in fig. 1(c), the pole is related to the internal node capacitance -which is in general a parasitic capacitance associated to MOST channel capacitance, but can be in some high-frequency current-

mode filters explicitly added-, whereas the zero is related to the feedforward capacitance between input and output node, and is physically due to the overlap capacitance between drain and gate of the output transistor. The effect of the right-half plane zero limits the maximum attainable Q factor in continuous-time current-mirror based filters [12].

Figure 2 (a) shows SPICE simulation results, based on a standard CMOS process, of a simple current mirror frequency response. The phase evolution in high frequency towards 180 degrees confirms the non-minimum-phase zero existence.

Apart from the simple mirror, the most widely used CMOS and bipolar current mirrors are the Wilson/improved Wilson mirror, and the cascode mirror. These mirrors are used to rise the poor low output impedance of the two-transistor mirror, either by means of feedback -Wilson- or using common-base cascoding techniques -Cascode-. The inclusion of added transistors give rise to a worsening in the bandwidth of the mirrors, but the shape of the response is essentially the same as the model in expression (2). The validity of the models holds, since it is physically related to first-order reduction of bandwidth due to channel capacitances and a certain feedforward effect.

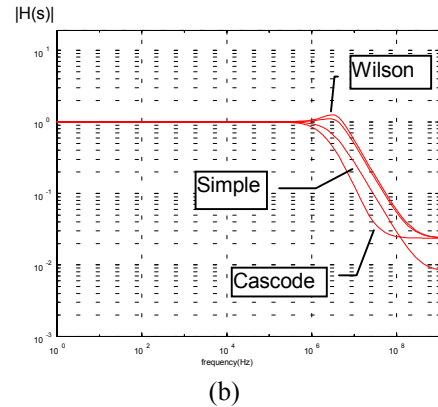
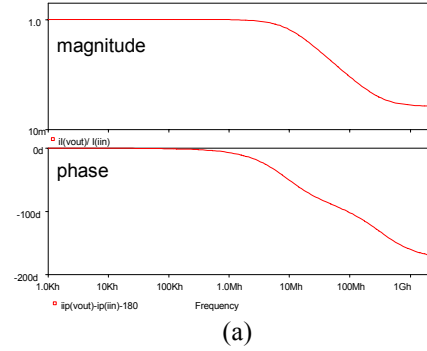


Figure 2. (a) SPICE simple current mirror frequency response simulation and (b) ISAAC frequency response comparison.

For the sake of completeness the response of the four types of mirrors are reproduced in table I. Nevertheless, as the comparison using symbolical analysis [7] shown in figure 2(b) presents, all the responses (from first order dynamics to third order dynamics) can be assimilated or modelled by the simpler and more general model in (2). Note that the simple and Wilson response expressions include only the mid-frequency effects, whereas the cascode expression includes also the RHP zero effect. If very fine modelling is desired -for instance in phase margin prediction, or in the phase error simulation in filters-, the slight peak shown by Wilson and improved Wilson mirrors might be seen as a problem. This resonance, due to the use of feedback at transistor level, corresponds to a complex pair of poles and zero with same real part and leads to a flatter phase response than a single pole response. This problem will be solved with the circuit-level implementation of the model in (2), as presented in section III.

<i>simple</i>	$\frac{g_m}{g_m + 2C_{gs}s}$
<i>Wilson and improved Wilson</i>	$\frac{g_m^2 + 2g_m C_{gs}s}{g_m^2 + 2g_m C_{gs}s + 2C_{gs}^2 s^2}$
<i>Cascode</i>	$\frac{g_m^3 + g_m^2 C_{gs}s - g_0 C_{gs}^2 s^2}{g_m^3 + 5g_m^2 C_{gs}s + 6g_m C_{gs}^2 s^2 + 2C_{gs}^3 s^3}$

Table 1. Common Mirrors Frequency Response

B. Effects of Reduction in Transistor Sizes

An objection to the previous proposed model is that the effect of the right-half plane zero is so above the frequencies of interest that its effect can be neglected. However, as long as the stability issue is concerned, the phase it introduces is added to the phase expected from the first-order analysis pole and therefore can distort a phase margin prediction. This statement becomes more important when the position of the zero shifts closer to the pole, and this happens when reducing transistors sizes; therefore further analysis is needed.

The reduction of size -towards submicron- is a natural tendency from a technological point of view, and it also benefits amplifier design, as it increases speed and bandwidth. The effect of decreasing transistors sizes over the capacitances of the model -from the designer's point of view and for a given technology-, is a reduction of the ratio between the zero and the pole, and hence an increase of the phase introduced by the zero.

If a parameter γ is defined as follows (3),

$$\gamma = \frac{\omega_Z}{\omega_P} = \frac{g_m / C_{gd}}{g_m / 2C_{gs}} = 2 \frac{C_{gd}}{C_{gs}} \quad (3)$$

and considering the relation of the gate-drain capacitance to the fixed overlap distance, and assuming the gate-source capacitance as the overlap capacitance and a portion of the parallel-plate channel capacitance given by (4),

$$\begin{aligned} C_{gd} &= C_{ol} = C_{ox} W_{eff} L_D \\ C_{gs} &= C_{ol} + C_{channel} = C_{ox} W_{eff} L_D + \frac{2}{3} C_{ox} W_{eff} (L - 2L_D) \end{aligned} \quad (4)$$

an expression for the parameter γ is derived (5) as a function of the channel length :

$$\gamma = 2 \left[\frac{C_{ox} W_{eff} L_D + \frac{2}{3} C_{ox} W_{eff} (L - 2L_D)}{C_{ox} W_{eff} L_D} \right] = -\frac{2}{3} + \frac{4}{3L_D} \cdot L(\mu) \quad (5)$$

The previous expression states that the shorter the transistor, the closer the zero is to the pole and thus, the modelling of the zero becomes more necessary.

C. Bipolar versus MOS technology current mirror modelling

In bipolar technology, the mid-frequencies response of the mirror can be derived [8] starting from the DC gain - which is different from unity due to base current errors- and substituting a frequency dependence of the current gain as in (6a).

$$h_{FE}(s) \cong \frac{\beta_0}{1 + s \beta_0 / \omega_T} \xrightarrow{\omega \gg \omega_T / \beta_0} \frac{\omega_T}{s} \quad (6a)$$

$$\frac{i_D(s)}{i_G(s)} \cong \frac{g_m}{C_{gs}} \cdot \frac{1}{s} \quad (6b)$$

In the frequency margin where the shaping is expected, h_{FE} can be approximated with an integrating response. On the other hand, although unity-gain frequency has an intuitive sense for bipolar devices, the gate displacement current in MOS transistors yields equation (6b), also an integrating characteristic. Therefore it is reasonable to assume that both bipolar and CMOS mirrors share qualitatively medium-frequency responses and thus, the proposed model is general. The HF feedforward zero due to feedforward is also present in both technologies. The following expressions (7) and simulations -figure 3- for the Wilson mirror illustrate these statements.

$$H_{\text{Wilson CMOS}}(s) = \frac{2C_{gs}g_m s + g_m^2}{2C_{gs}^2 s^2 + 2C_{gs}g_m s + g_m^2} \cdot (1 - s/\omega_Z) \quad (7a)$$

$$H_{\text{Wilson bipolar}}(s) = \frac{(2/\omega_T)s + 1}{(2/\omega_T^2)s^2 + (2/\omega_T)s + 1} \cdot (1 - s/\omega_Z) \quad (7b)$$

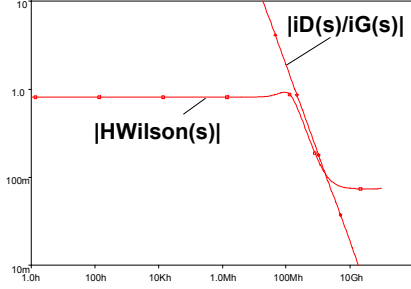


Figure 3. CMOS Wilson mirror response and drain/gate current transfer.

D. Other current mirror types

Apart from the aforementioned four types of current mirrors, several modifications have been proposed to enhance their performance. One example is the high-frequency compensated mirror used in [9], shown in figure 4(a). Since the 1-pole 1-zero model is related to capacitances inherent to technology and common to each mirror, the model is valid, as simulations in figure 4(b) confirm.

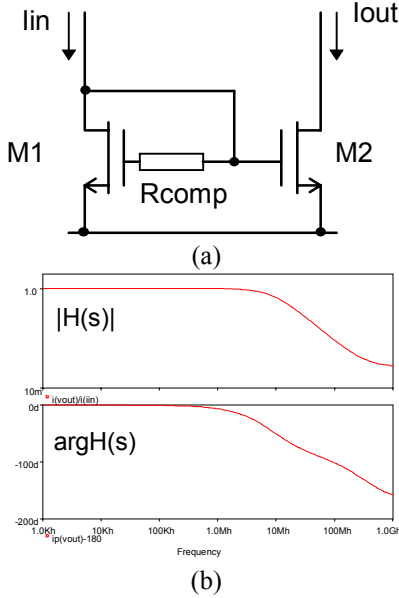


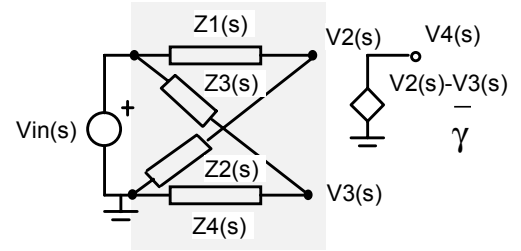
Figure 4. (a) High frequency compensated mirror [9] and (b) simulated frequency response.

In addition to this, the model is still valid for current mirrors designed for low-power subthreshold region operation, although they are not intended for high-frequency applications. On the other hand, the model is not suitable for dynamic mirrors, because of their sample-domain nature, this requires for the switching frequency to be lower than the first-order pole of the mirror in order to properly operate.

III. CIRCUIT-LEVEL MODELLING

The proposed model finds application when included in existing or extracted macromodels of amplifiers. In particular, it is useful in current-mode amplifiers, namely, CCIIs and CFAs. The inclusion of the model is needed to predict the right amount of instability of the design.

One approach of circuit-level inclusion of the analytical model in a macromodel may be to use the circuit in fig. 1(c), closely related to the actual mirror. However, a lattice network is a circuit which models a non-minimum phase zero, and is easier to add to a macromodel. Figure 5 shows the lattice network -shaded- and its general response.



$$V_o(s) = V_{in}(s) \left(\frac{Z_2(s)}{Z_1(s) + Z_2(s)} - \frac{1}{\gamma} \frac{Z_4(s)}{Z_3(s) + Z_4(s)} \right)$$

Figure 5. Lattice network with zero shifter and its general frequency response.

Substituting the impedances by resistors and capacitors (8a), the network introduces a zero and a pole at the same frequency. Using a controlled source to shift the position of the zero, the response is described after (8b).

$$\left. \begin{aligned} Z_1(s) &= R \\ Z_2(s) &= 1/Cs \end{aligned} \right\} LPF, \quad \left. \begin{aligned} Z_3(s) &= 1/Cs \\ Z_4(s) &= R \end{aligned} \right\} HPF \quad (8a)$$

$$\frac{V_4(s)}{V_1(s)} = \frac{\gamma - RCs}{\gamma + \gamma RCs} \Leftrightarrow \left\{ \begin{aligned} H(0) &= 1 \\ \omega_p &= \frac{-1}{RC}, \omega_z = \frac{\gamma}{RC} \end{aligned} \right\} \quad (8b)$$

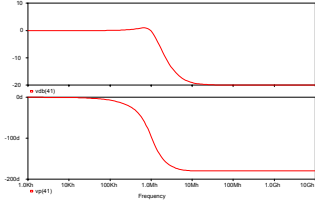


Figure 6. Simulation of the frequency response of a lattice network with resonant branches.

where γ has the same meaning as previously defined (3). One advantage of using the lattice network is that, with the inclusion of series RLC impedances in each branch, the response obtained is resonant as that of the commonly used Wilson mirrors (figure 6 simulation). This approach should be used if an accurate modelling of the phase response -flatter- is needed.

IV. APPLICATION TO PHASE MARGIN PREDICTION

As an example of application of the proposed current mirror model, the obtention of the phase margin in a closed loop CFOA is presented. The stability issue is a key factor in these high-speed devices, since they are operated close to their maximum frequency limits [10]. Some specialists' macromodels have included a three pole model for the open loop gain (transimpedance) [11], being the higher frequency pole needed to properly account for the phase lag actually introduced by the non-minimum phase zero.

Figure 7 shows qualitatively the error introduced in the phase margin when the high frequency zero is neglected in analysis or simulation.

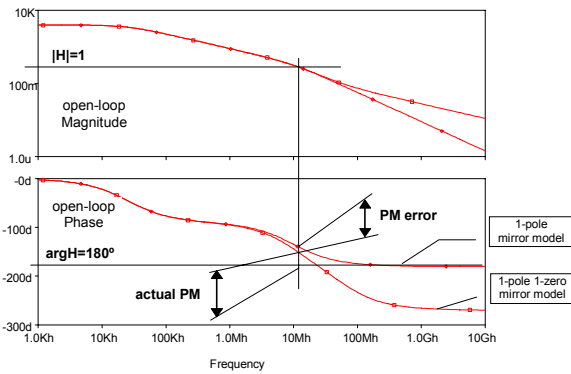


Figure 7. (a) Phase margin error due to neglecting the non-minimum-phase zero

From a quantitative point of view, the effect of the HF zero over the simple pole model can be interpreted as a decreasing in phase margin, or, in other terms, the existence of a virtual lower frequency pole, expressed as ω_V . The phase of the virtual pole equals that of both actual pole and zero, yielding

$$\tan^{-1}\left(\frac{\omega}{\omega_P}\right) + \tan^{-1}\left(\frac{\omega}{\gamma(L)\omega_P}\right) = \tan^{-1}\left(\frac{\omega}{\omega_V}\right) \quad (9)$$

Hence, with the assumption that $\omega = \omega_P$, the ratio first-pole/virtual pole is given by

$$\frac{\omega_P}{\omega_V} = \tan\left(\frac{\pi}{4} + \tan^{-1}\left(\frac{1}{\gamma(L)}\right)\right) \quad (10)$$

This expression is useful since, for a two-pole open-loop response, the phase margin -or equivalently damping factor- can be written as

$$\frac{f_p}{\text{GBW}} = 2\zeta = \frac{\sin^2(\text{PM})}{\cos(\text{PM})} \quad (11)$$

Therefore, the relative error in the damping factor, due to the exclusion of the HF zero is given by

$$\varepsilon_\zeta = \frac{\Delta\zeta}{\zeta} = \frac{\zeta_{\text{error}}}{\zeta_{\text{real}}} - 1 = \frac{\omega_P}{\omega_V} - 1 = \tan\left(\frac{\pi}{4} + \tan^{-1}\left(\frac{1}{\gamma(L)}\right)\right) - 1 \quad (12)$$

As expected from equation (5), this error increases when reducing the transistor length.

As an example of use, the simulated transistor-level phase margin of a unity-gain follower based on a CMOS CFOA results in 26.7° (with minimum-size transistors in current mirrors acting as supply current sensing circuits). The simulated phase margin with the proposed current mirror model is essentially the same if it is properly adjusted, while a single pole model overestimates the phase margin to 35.14° . Taking into account other additional sources of instability, this 30 % error can hide potentially unstable circuit configurations.

V. CONCLUSIONS

A general frequency model of current mirrors has been presented. The model accounts for first-order frequency effects -modelled with one pole-, and a high-frequency non-minimum phase zero, due to feedforward capacitance. The model is suitable for several types of mirrors and is valid regardless of the implementation technology. The described circuit-level implementation of this model can be of practical use, as it has been proven to be useful for its inclusion in the design and phase margin prediction of high-frequency amplifiers.

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