An Asynchronous Finite State Machine Controller for Integrated Buck-Boost Power Converters in Wideband Signal-Tracking Applications

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Abstract—In this paper, a simple, fully digital, asynchronous finite state machine controller for buck-boost power converters is introduced and simulated. With the addition of only two analog voltage comparators and six power MOS switches, the circuit can generate an output voltage that is able to track a dynamic reference with a 1 MHz bandwidth with good efficiency using a 0.35 μm CMOS process. The controller also provides adiabatic charging and discharging of capacitive loads.

I. INTRODUCTION

In telecommunications and computing systems, the continuous trend in miniaturizing power processing subsystems, which are in charge of guaranteeing high efficiency in the use of supply energy, stands from the global system-level impact of those subsystems in terms of volume and weight, and thus on portability. This statement is particularly true for current and future generation systems-on-chip (SOC), a trend which provides a line of convergence for the implementation of systems for portable, mobile and autonomous applications, in which power management is one of the key performance limiting factors as regards to ergonomics and operability time. The ultimate step consequently consists in the fully monolithic integration of the power converter together with the same circuits which constitute its load [1–4].

On-chip efficient power management circuits usually focus on integrating a regulator, a circuit which pursues a stable output regardless of perturbations in both the output load and input power source. There are indeed a few challenging applications in which the output of the converter is forced to track a wideband time-varying signal. Among the different applications for such wideband amplifiers, we could point out three cases with stringent specifications, namely A) MEMS-based capacitive actuators, where the positive-feedback pull-in effect can be overcome applying time-variable supply, B) System-level optimization of power consumption in digital circuits, via Adaptive Voltage Scaling scheme (AVS) [5, 6], C) Envelope Elimination and Restoration (EER) or Kahn technique [7, 8], which theoretically allows implementation of linear highly efficient RF Power Amplifiers (as required by RF power amplification in modern digital modulations such as in EDGE and UMTS as well as in WiLAN and 4G applications that exhibit significant envelope modulation by adaptively supplying the RF PA with the wideband baseband envelope signal via a switching power converter, of the type usually applied to efficient DC-DC conversion. One of the key remaining challenges for a successful realization of such systems is the practical implementation of the efficient, wide-bandwidth tracking power converter.

Independently of whether the power converter operates in a regulator or amplifier application, one additional challenge is that of designing the control scheme and modulation law to drive the converter [9]. Recently, feasibility of practical high-frequency, high-performance digital controllers for DC-DC applications has been demonstrated [10]. Based on custom VLSI realizations of the key building blocks, including high-resolution high-frequency digital pulse-width modulators (DPWM), simplified discrete-time compensator schemes, and A/D converters, such controllers can offer the advantages of lower sensitivity to parameter variations, programmability, and reduction or elimination of external passive components, without compromising dynamic performance, simplicity or cost [11–13].

Application of digital controllers in the field of power converters frequently rise problems regarding efficiency due to their power consumption. One of the causes is the requirement of a very low latency synchronous digital circuit, which implies high-frequency clock signals routed system-wide (thus highly capacitively loaded) that are continuously dissipating power.

On the contrary, since asynchronous digital controllers are clockless, they have a very low power consumption as opposed to synchronous controllers [14] and an extremely low latency (they don’t need to wait one clock period to change their internal state). Clock elimination avoids the need of buffers to reduce clock skew as well as electromagnetic interference [15]. Despite all those advantages, asynchronous design is more complex and there are still few design tools to ease the task.

Asynchronous digital circuits are usually described with a Finite State Machine model or FSM [16]. Asynchronous finite state machines are referred as AFSM. This description provides a graphical and simple representation of the behavior of small and medium size digital sequential systems.

This paper focuses on the on-chip integration of a switching power converter targeting wideband tracking application using asynchronous digital control. In Section II the power converter architecture is presented. In Section III the AFSM controller architecture and implementation is explained in detail and in Section IV the simulation results are shown.

II. SYSTEM ARCHITECTURE

The the non-inverting buck-boost power converter schematic is shown in figure I [17–20]. The input voltage is connected to $V_{IN}$ and the output voltage is available in $V_{OUT}$. $C_L$ and $R_L$ model the load and the inductor acts as an energy transfer element. $M_1$, $M_2$, $M_3$, $M_4$, $M_5$, $M_6$ and $M_7$ are power MOS transistors and all the others are small MOS switches. The gate voltage $V_{GS}$ of the MOS transistors are logically driven directly by the AFSM controller. The switch $M_1$ was implemented as a pass gate instead of a single PMOS transistor in case of $V_{OUT}$ is required to go below the PMOS threshold voltage.
The running sequence generated by the AFSM controller depends on a comparator that detects whether \( V_{OUT} \) is below or above a reference or desired voltage \( V_{REF} \). The AFSM controller also requires to know the inductor current sign and if the inductor current reaches a certain limit \( I_{LIM} \). This current can be measured indirectly by monitoring the voltage drop of either \( V_{DS3} \) if \( M_2 \) is on or \( V_{DS3} \) if \( M_3 \) is on. The voltage is compared either with zero if the sequence requires to detect when the inductor is discharged or with a constant positive voltage \( V_{LIM} \) if the sequence requires to detect when its current reaches a certain limit. \( V_{LIM} \) is related to the inductor current limit \( I_{LIM} \) by means of

\[
V_{LIM} = I_{LIM}R_{ON}
\]

where \( R_{ON} \) is the on resistance of \( M_2 \) or \( M_3 \) switches. Since the controller only requires to know either the current sign or current limit at each state, a simple multiplexing circuit is used, implemented by \( M_{2b}, M_{3b}, M_5 \) and \( M_6 \). This way, allowing a single comparator to perform all current detection of the inductor reduces the power consumption and thereby increases efficiency. Despite two additional control signals are needed, namely \( V_{G6} \) and \( V_{G7} \), they can be easily generated by the AFSM controller.

III. THE FINITE STATE MACHINE CONTROLLER

A. Architecture

The AFSM controller diagram is shown in figure 2, where the circles represent major states. The state names and their function are summarized in the following list:

- \( \text{ChgL} \) charges the inductor until its current reaches the specified limit \( I_{LIM} \). When this happens, the state jumps to \( \text{LtoC} \). Active transistors are \( M_1, M_3, M_{3b} \) and \( M_6 \).
- \( \text{LtoC} \) transfers energy from the charged inductor to the output load. If the output voltage reaches the reference, it jumps to \( \text{LtoV} \) to return the remaining energy of the inductor to the source. If the inductor discharges completely without the output voltage reaching the reference, the state jumps to \( \text{ChgL} \) to begin another charging cycle. Active transistors are \( M_2, M_{3b}, M_{4s} \) and \( M_7 \).
- \( \text{LtoV} \) returns the remaining inductor energy (if any) to the source. When it is done, it jumps back to \( \text{ChgL} \) if the output voltage is below the reference or to \( \text{CtoL} \) if it is above. Active transistors are \( M_2, M_{3b}, M_5 \) and \( M_7 \).
- \( \text{CtoL} \) transfers energy from the capacitor to the inductor, thus decreasing the output voltage, until it reaches the reference or the inductor current reaches a limit. Then it jumps to \( \text{DisL} \). Active transistors are \( M_2, M_{3b}, M_5 \) and \( M_6 \).
- \( \text{DisL} \) returns energy to the source. When it is done it jumps to \( \text{CtoL} \) if the output voltage is still above the reference or to \( \text{ChgL} \) if not. Active transistors are \( M_1, M_3, M_{3b} \) and \( M_7 \).

Each state is divided in two or three substates to implement a dead-time in the outputs to avoid current shoot across the MOS switches. The duration of the deadtime is taken from the constant time response of a chain of starving inverters. This solution provides a wide tuning range while keeping a very low power consumption. Another chain of starving inverters implement a stabilization time delay that the AFSM must wait just after entering in a new state before it can change of state again. This is necessary to avoid anomalous behaviors due to the nonzero response time of the comparators.

B. Implementation

The AFSM was coded in Verilog directly at gate level to avoid hazards or glitches caused by the logical simplifications done by the commercial available synthesizers, while allowing the possibility of automatic layout drawing. Glitches or hazards are acceptable on synchronous design as long as they disappear before the next clock
event, however, they increase the power consumption and can cause unwanted switching of the output transistors of the power converter, thereby decreasing efficiency. Also, they are a major cause of errors in asynchronous design, as glitches cannot be easily distinguished from real transitions in most of the asynchronous implementations.

In order to ease the design task and reduce the risk of glitches in the outputs, each state is implemented by using gate-level descriptions of generalized C-elements (gC) [21] and some simple additional logic. gC-elements are a type of latch with decoupled set and reset inputs. The state transition table of the gC-element is shown in table I and a gate level implementation, similar to those published in [22], in figure 3.

Each of the five states has, at least, a set and a reset signal. Their set signal is generated by performing a logical AND operation between the output of the substate from the controller can jump from and the jump condition itself, while their reset signal is generated by performing a logical OR operation of the outputs of the substates to the controller can jump to. The circuit has also an external global reset signal.

### IV. Results

The circuit was simulated at transistor-level with Spectre in the AMIS C035U 0.35 μm CMOS process and it will be manufactured in the near future. The width of the power MOS transistors has been set in order to have a $R_{ON}$ resistance of 0.5 Ω. The inductor parasitic resistance was set to 0.2 Ω based on a commercially-available inductor datasheet. The AFSM controller netlist has been implemented using standard cells of the digital library provided with the design kit to allow automatic layout routing.

In figure 4 the output voltage for some values of the reference voltage is shown. The efficiency reaches 75% for $V_{REF} = 3.3$ V and the circuit parameters of the figure. Peak efficiency was found to be beyond 80%. The ripple that can be observed for high output voltages is due to the discharge of the output capacitor by the resistive load, and can be easily reduced increasing the size of the output capacitor. The output ripple that can be observed for low output voltages is, however, due to the nonzero time response of the comparators and the controller, which cause a delayed controller state change.

Figure 5 shows the behavior of the power converter for a dynamic input reference, consisting in a 1 MHz triangular wave. The value of the gate voltages of the power transistors and current drained from the input $V_{IN}$ are also shown in order to assess the behavior of the controller. Although it might seem that the tracking error is high, an improved topology based on the linear-assisted scheme can be applied in this case, thus increasing the overall efficiency of the system.

The effect of the delay of the comparators and the controller is an output voltage going slightly above the reference at the end of the $LtoC$ state during the rising edge of the triangle input waveform and going slightly below the reference at the end of the $CtoL$ state during the falling edge. Those effects are expected to be much smaller with faster deep submicron technologies. Also, if at least one more bit of information about the difference between output voltage $V_{OUT}$ and the reference $V_{REF}$ is made available to the controller, the inductor could be charged with less energy during the $ChgL$ state if this difference is small, making the charging of the output capacitor during $LtoC$ state much slower and reducing the effect of a slow circuitity at the output voltage. This will also increase efficiency since it will reduce the amount of remaining energy that has to be returned to the source during the $LtoV$ state. Moreover, if the load is mainly capacitive, the controller could be stopped if the difference is small enough.

### V. Conclusion

In this paper we have shown the suitability of asynchronous digital controllers for power converters. We also have presented a simple AFSM controller for buck-boost power converters with the capability of adiabatic charging and discharging of capacitive loads and found its main limitations, which are related to the circuit latency. Simulated response indicates 75% efficiency with a 8.5 MHz switching frequency in a 0.35 μm CMOS process technology. Both bandwidth and efficiency is expected to increase with advanced submicron technologies, while output ripple is expected to decrease. The AFSM netlist description in Verilog and a minimal analog circuitry allows for easy portability of the design amongst different manufacturing processes, for automatic layout generation and routing of the controller from a library of standard digital cells and also for reducing the design cycle or time to market of products which require power converters.

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### Table I

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<thead>
<tr>
<th>S</th>
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<tr>
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<td>0</td>
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<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
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Figure 3. Generalized C-element gate-level implementation. $S$ is the set signal, $R$ is the reset signal and $Q$ is the output.
The presented circuit can be used in environments where a high frequency output is required, such as Adaptive Voltage Scaling (AVS) and Envelope Elimination and Restoration (EER) or in applications where the load has a significant capacitive component, such as in MEMS capacitive actuator driving or also as a simple and fast replacement of classic inductor-based power converters.

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